ECE 340 Lecture 35
Semiconductor Electronics

Spring 2022
10:00-10:50am
Professor Umberto Ravaioli
Department of Electrical and Computer Engineering
2062 ECE Building

Today's Discussion

- **Realistic Threshold model**
- **The MOS Field Effect Transistor**
- **Output Characteristics**
- **Transfer Characteristics**

Real Surface effects – Work function difference

- **We assumed in the previous analysis for simplicity**

$$\Phi_m = \Phi_s$$

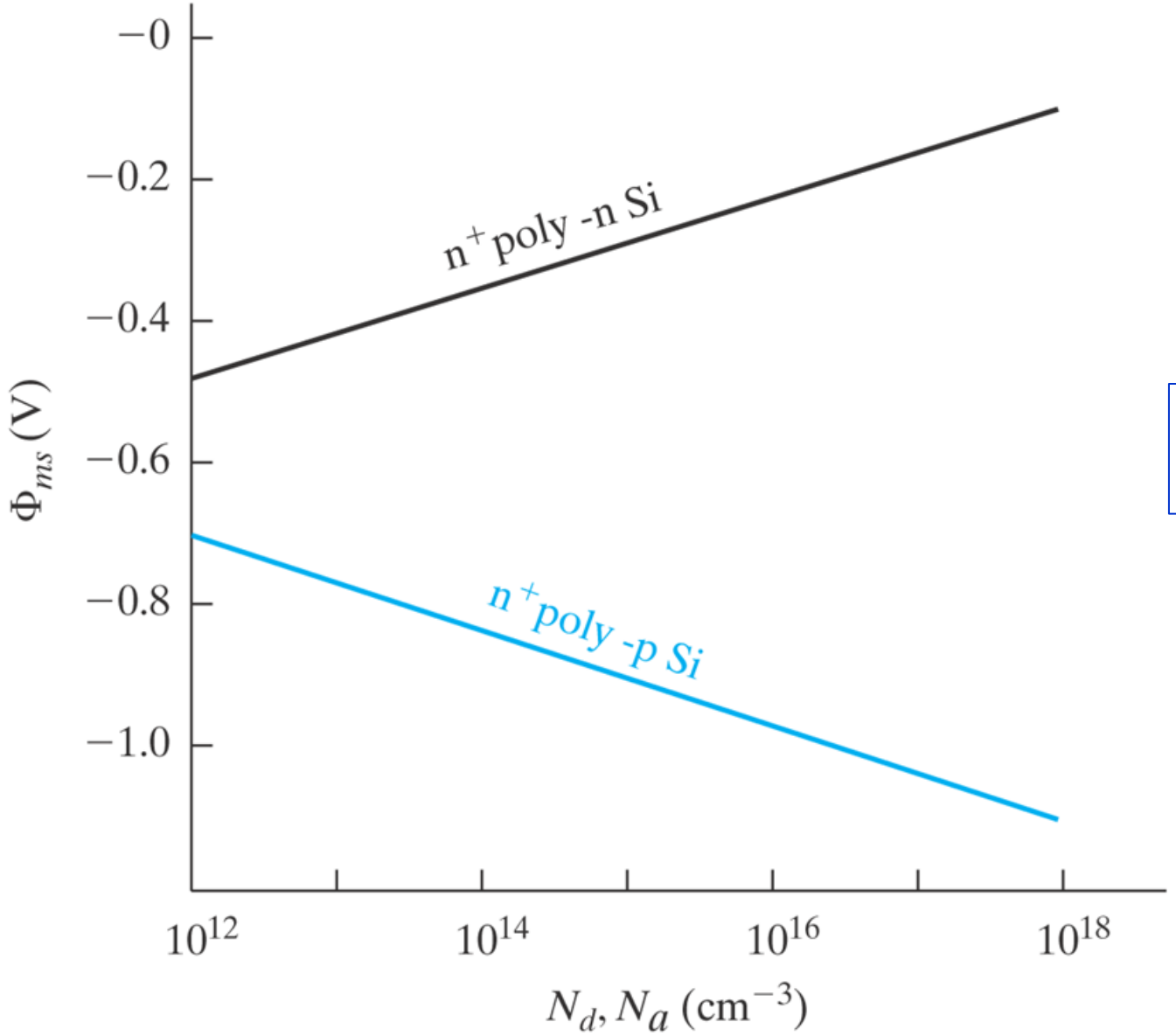
- **In general, we are limited in the choice of metal by technological constraints and**

$$\Phi_m \neq \Phi_s$$

- **It is convenient to define the quantity**

$$\Phi_{ms} = \Phi_m - \Phi_s$$

n+ plus polysilicon for gate electrode

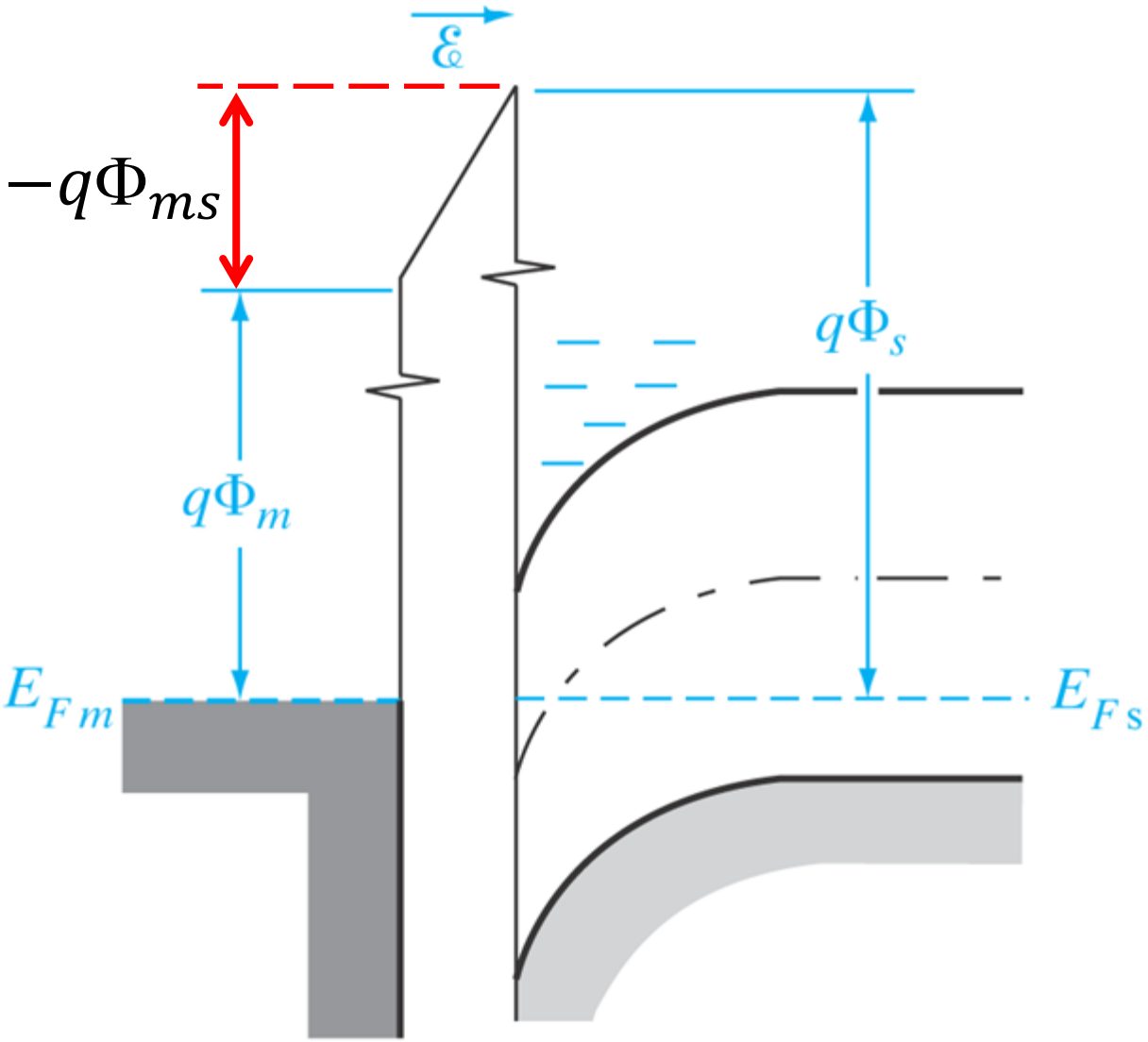


common choice

instead of metal

$$\Phi_{ms} < 0$$

Effect of negative workfunction difference

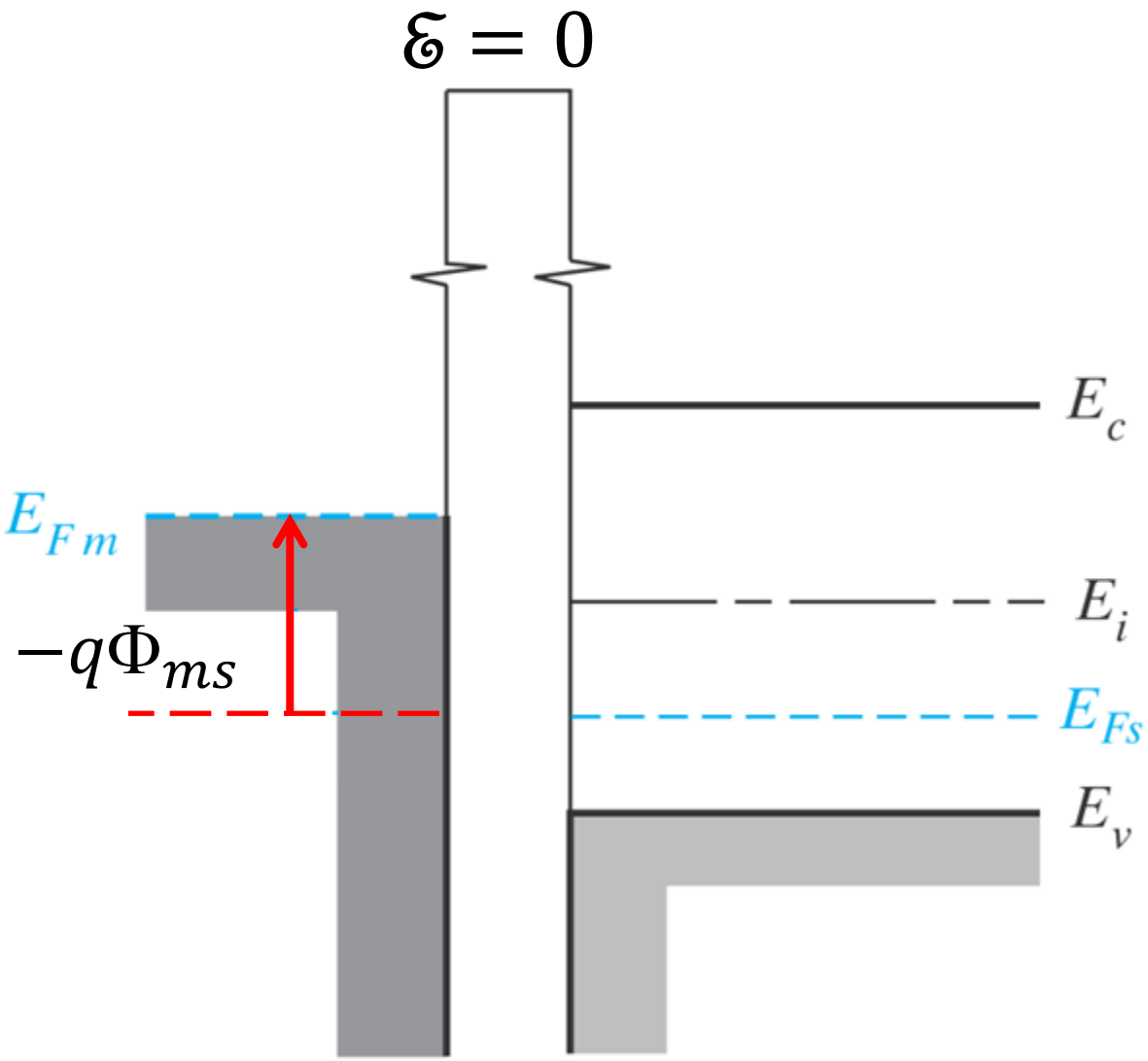


EQUILIBRIUM

$$V = 0$$

$$\Phi_{ms} < 0$$

Apply $V_{FB} = \Phi_{ms}$ to obtain flat band



FLAT BAND

$$V = V_{FB} = \Phi_{ms}$$

$$\Phi_{ms} < 0$$

Real Surface effects – Interface charge (1)

- **Alkali metal ions (e.g. Na^+) inside the oxide cause a mobile charge Q_m inducing negative charge in Si (reduced by careful processing)**

- **Imperfections in the SiO_2 material cause positive trapped charges Q_{ot} ($\approx 10^{10}\mathrm{cm}^{-3}$).**

Real Surface effects – Interface charge (2)

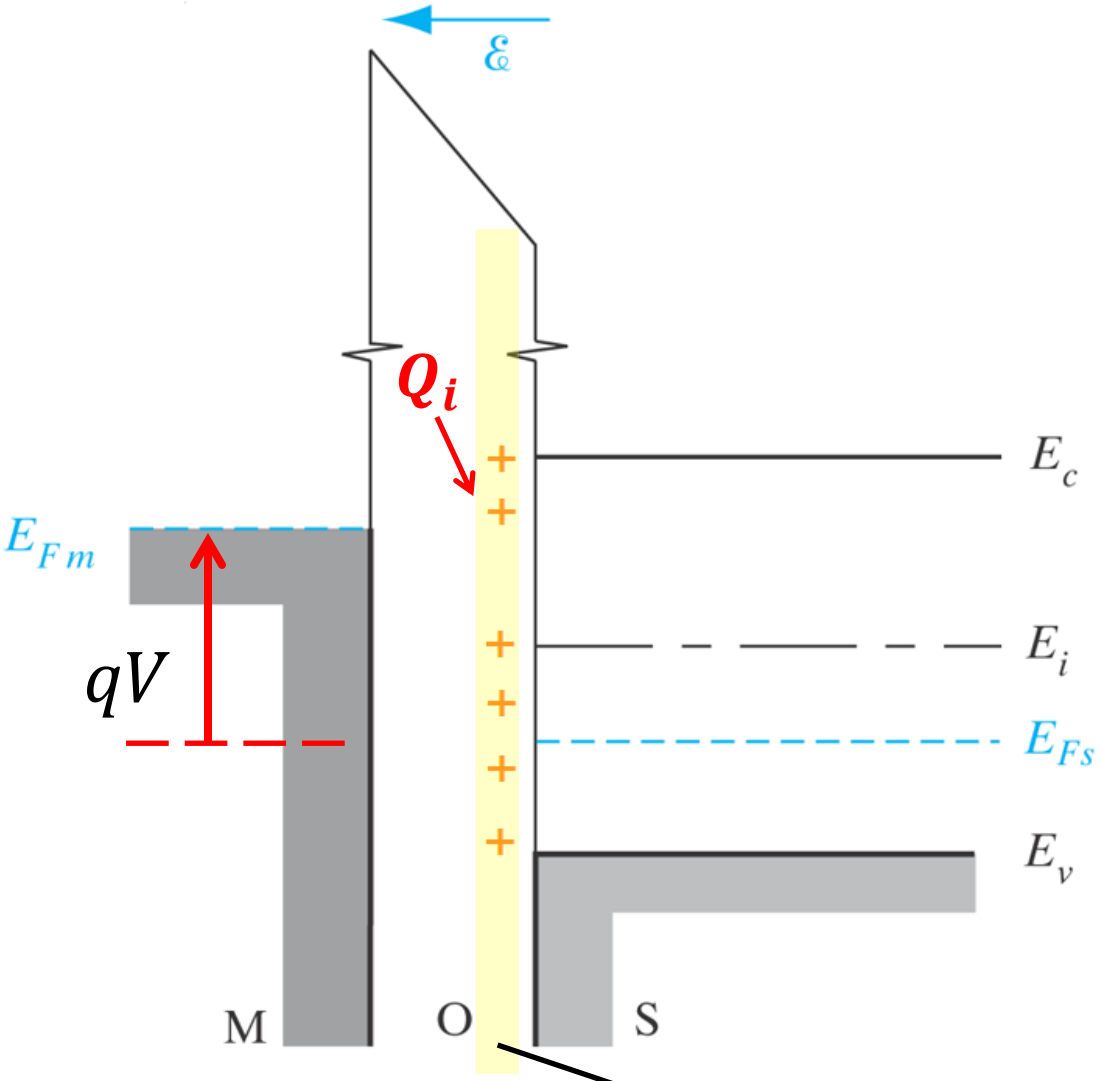
- **Positive fixed charges Q_f in a transition layer at the interface.**

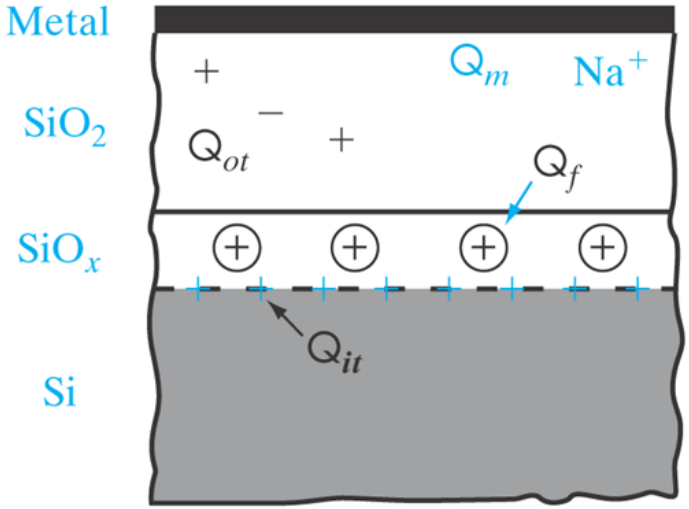
- **Positive charges Q_{it} at the Si- SiO_2 interface (interface states) due to mismatch causing "ionic" Si atoms with incomplete bonds.**

$$Q_{it} + Q_f \approx 10^{10}\,\mathrm{cm}^{-3}$$ **[100]** *preferred for devices*

$$Q_{it} + Q_f \approx 10^{11}\,\mathrm{cm}^{-3}$$ **[111]**

Effect of interface charge

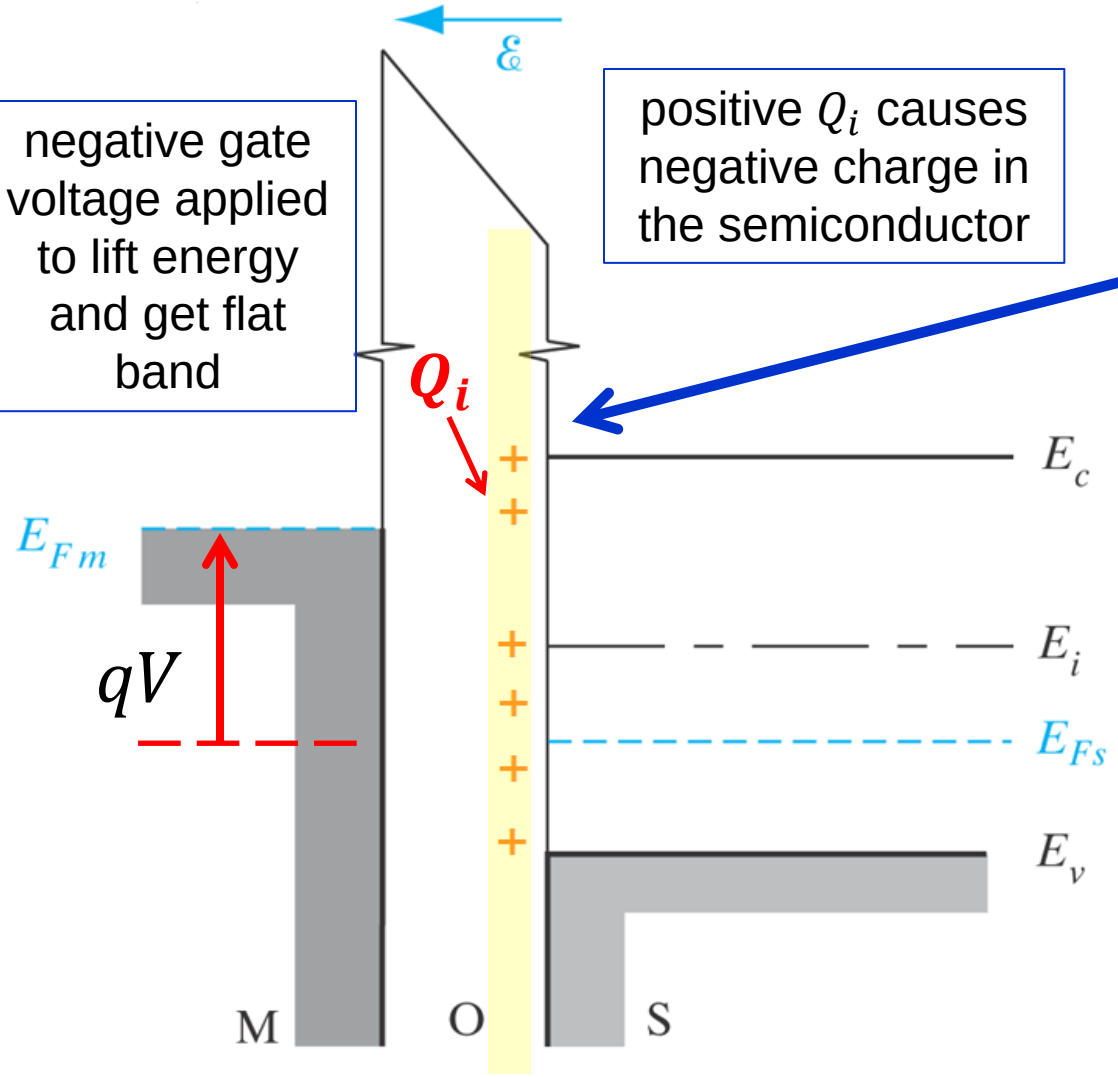




$$V = V_{FB} = -\frac{Q_i}{C_i}$$

Equivalent sheet of charge Q_i at the interface **accounting for all**

Effect of interface charge



negative gate voltage applied to lift energy and get flat band

positive Q_i causes negative charge in the semiconductor

Electric displacement $\varepsilon\mathcal{E}$ discontinuity because of interface charge

$$\varepsilon_{ox}\mathcal{E}_{OX} - \varepsilon_s\mathcal{E}_S = \rho_i$$

$$V = V_{FB} = -\frac{Q_i}{C_i}$$

Threshold Voltage

Ideal case

$$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

Threshold Voltage

Work function difference

Interface charge

Depletion layer charge

Strong inversion condition

Enhancement and Depletion MOSFET

- **Enhancement-mode MOS usually employed for switching elements. These devices are off (no channel) at zero gate–source voltage.**

- **Depletion-mode MOS, usually employed to realize “resistors” in logic circuits. These devices are normally on (already with a channel) at zero gate–source voltage.**

Exercise – Characterize MOS structure

- ***n*-channel MOS on *p*-type Si substrate doped with**

$$N_A = 5 \times 10^{15}\ \mathrm{cm}^{-3}$$

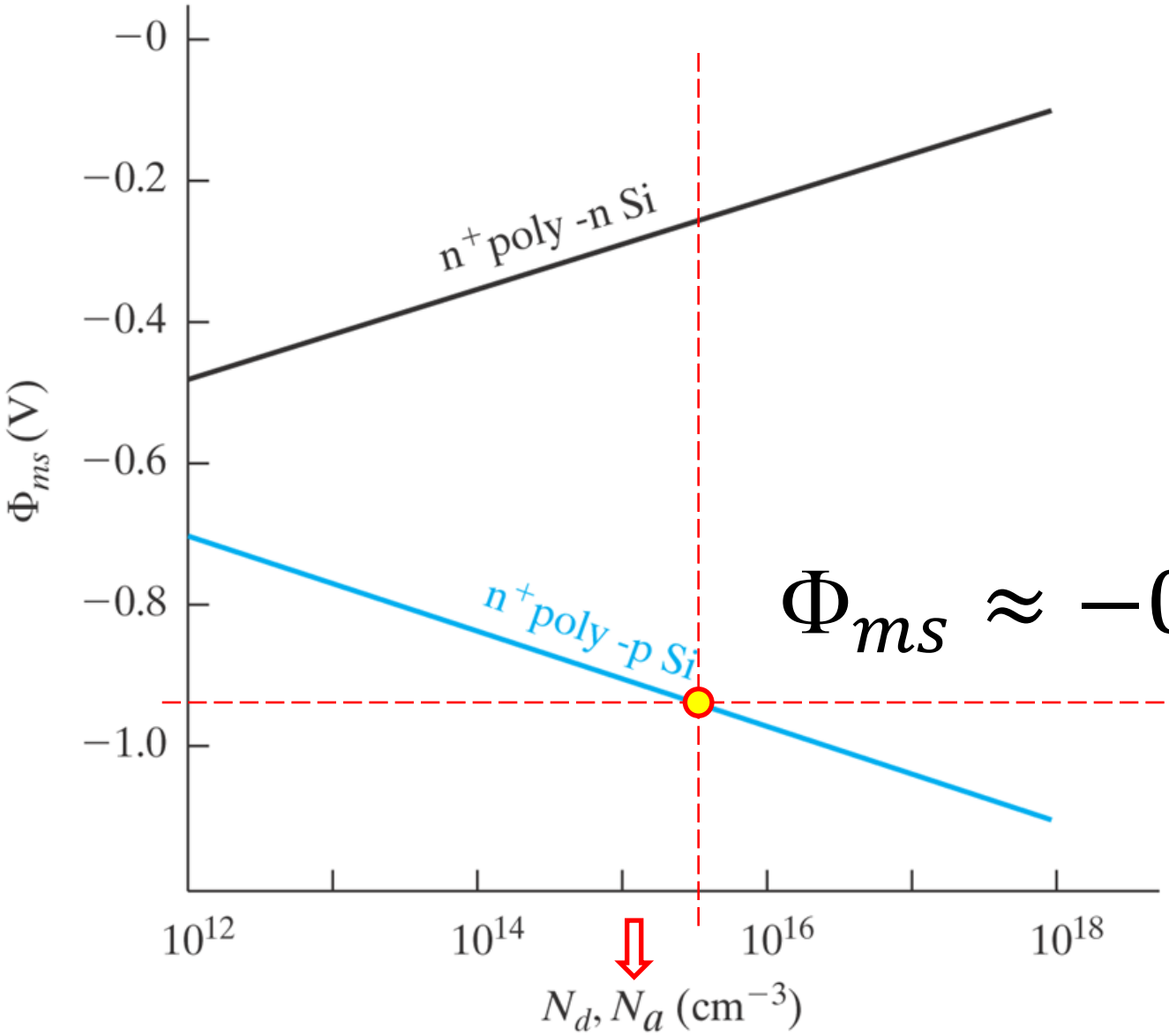
- **n^+ poly-silicon gate**
- **Gate oxide thickness**

$$d = 100\text{Å}$$

- **Effective interface charge**

$$Q_i = 4 \times 10^{10} q\ \mathrm{C/cm}^2$$

Exercise



$$\Phi_{ms} \approx -0.95\ V$$

Exercise

Interface Charge

$$Q_i = 4 \times 10^{10} q \text{ C/cm}^2$$

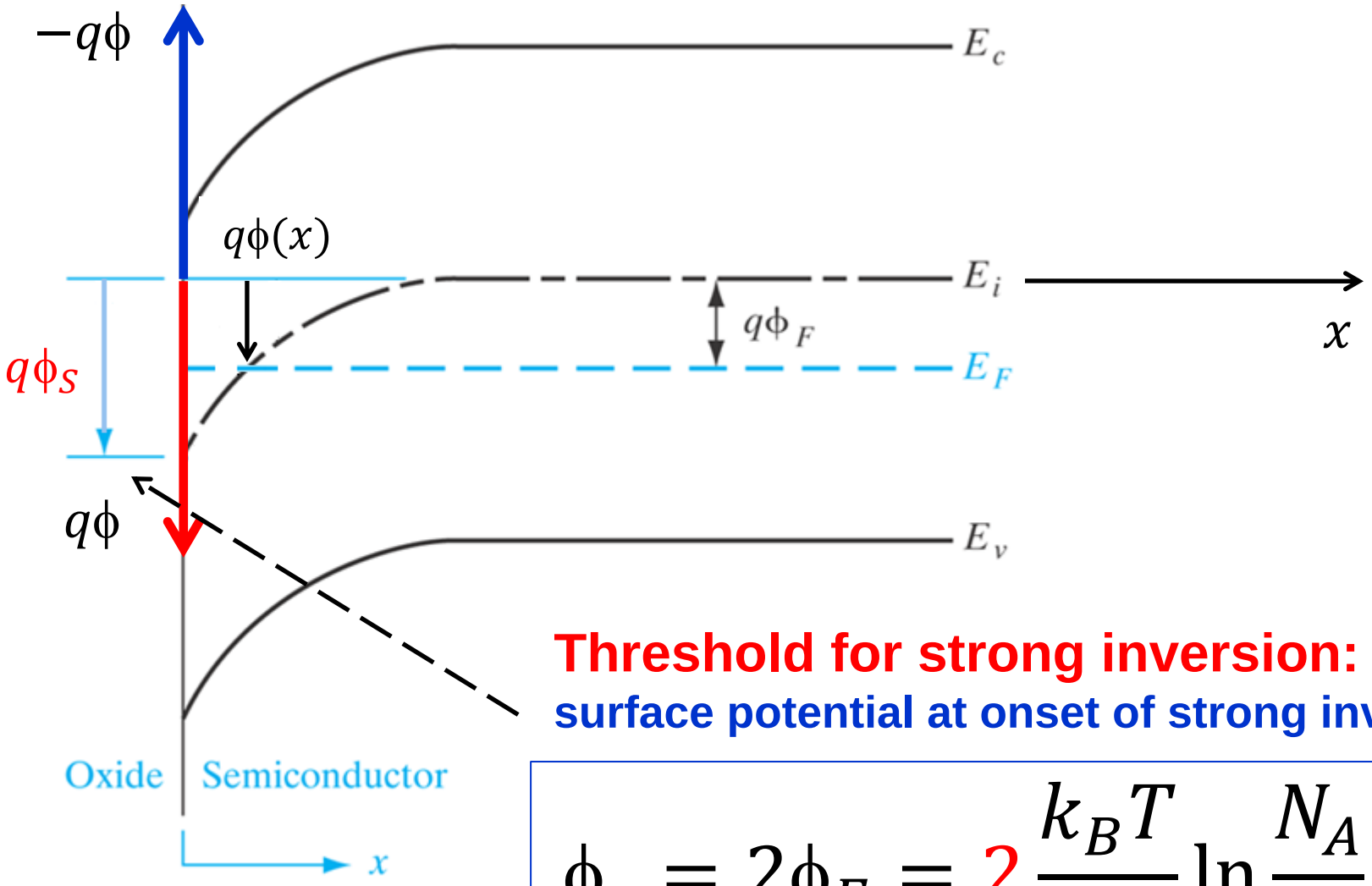
$$= 4 \times 10^{10} \times 1.6 \times 10^{-19} = 6.4 \times 10^{-9} \text{ C/cm}^2$$

Oxide Charge $d = 100\text{Å} = 10^{-8}\text{m} = 10^{-6}\text{cm}$

$$C_i = \frac{\varepsilon_i}{d} = \frac{3.9 \times 8.85 \times 10^{-14}}{10^{-6}} = 3.45 \times 10^{-7} \text{ F/cm}^2$$

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i} = -0.95 - \underbrace{\frac{6.4 \times 10^{-9}}{3.45 \times 10^{-7}}}_{0.019\text{V}} = -0.969\text{V}$$

Reminder: strong inversion condition



Threshold for strong inversion:

surface potential at onset of strong inversion

$$\phi_s = 2\phi_F = 2\frac{k_B T}{q}\ln\frac{N_A}{n_i}$$

Exercise

$$\phi_F = \frac{k_B T}{q} \ln \frac{N_A}{n_i} = 0.0259 \times \ln \frac{5 \times 10^{15}}{1.5 \times 10^{10}} = 0.329\text{V}$$

Maximum Depletion Width at Threshold

$$W_{max} = \sqrt{\frac{2\epsilon_s 2\phi_F}{qN_A}} = 2\left(\frac{11.8 \times 8.85 \times 10^{-14} \times 0.329}{1.6 \times 10^{-19} \times 5 \times 10^{15}}\right)^{\frac{1}{2}}$$

$$= 4.15 \times 10^{-5}\ \text{cm} = 0.415\ \mu\text{m}$$

Depletion Charge at Threshold

$$Q_d = -qN_A W_m$$

$$= 1.6 \times 10^{-19} \times 5 \times 10^{15} \times 4.15 \times 10^{-5} =$$

$$= -3.32 \times 10^{-8}\ \text{C/cm}^2$$

Exercise

Threshold Voltage

$$V_T = V_{FB} - \frac{Q_d}{C_i} + 2\phi_F$$

$$= -0.969 - \frac{3.32 \times 10^{-8}}{3.45 \times 10^{-7}} + 0.658 =$$

$$= -0.215\text{V}$$

Exercise

Depletion Capacitance at Threshold

$$C_i = 3.45 \times 10^{-7} \frac{\text{F}}{\text{cm}^2} \quad \text{(found earlier)}$$

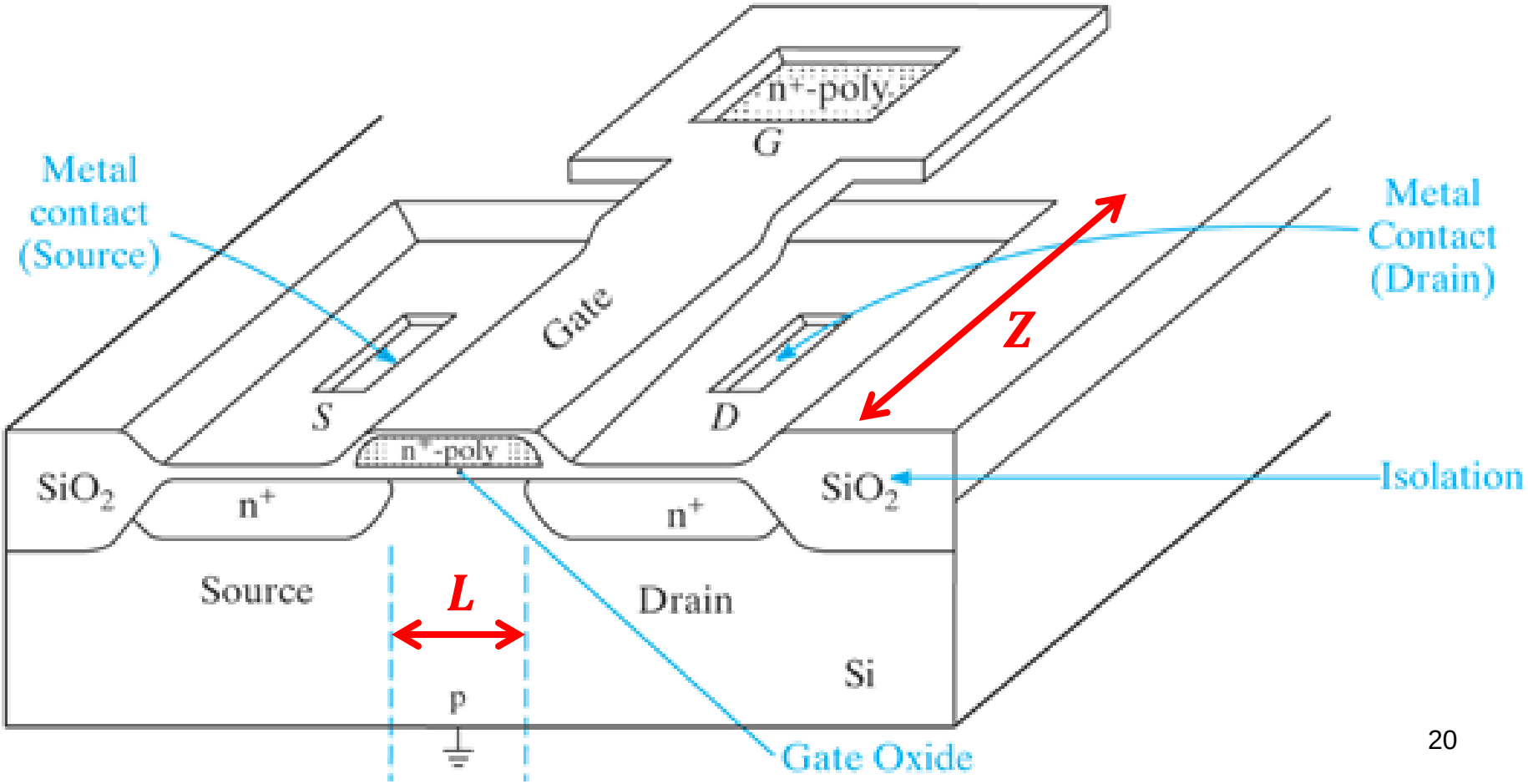
$$C_d = \frac{\epsilon_s}{W_{max}} = \frac{11.8 \times 8.85 \times 10^{-14}}{4.15 \times 10^{-5}} = 2.5 \times 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

$$C_{min} = \frac{C_i C_d}{C_i + C_d} = \frac{3.45 \times 10^{-7} \times 2.5 \times 10^{-8}}{3.45 \times 10^{-7} + 2.5 \times 10^{-8}} =$$

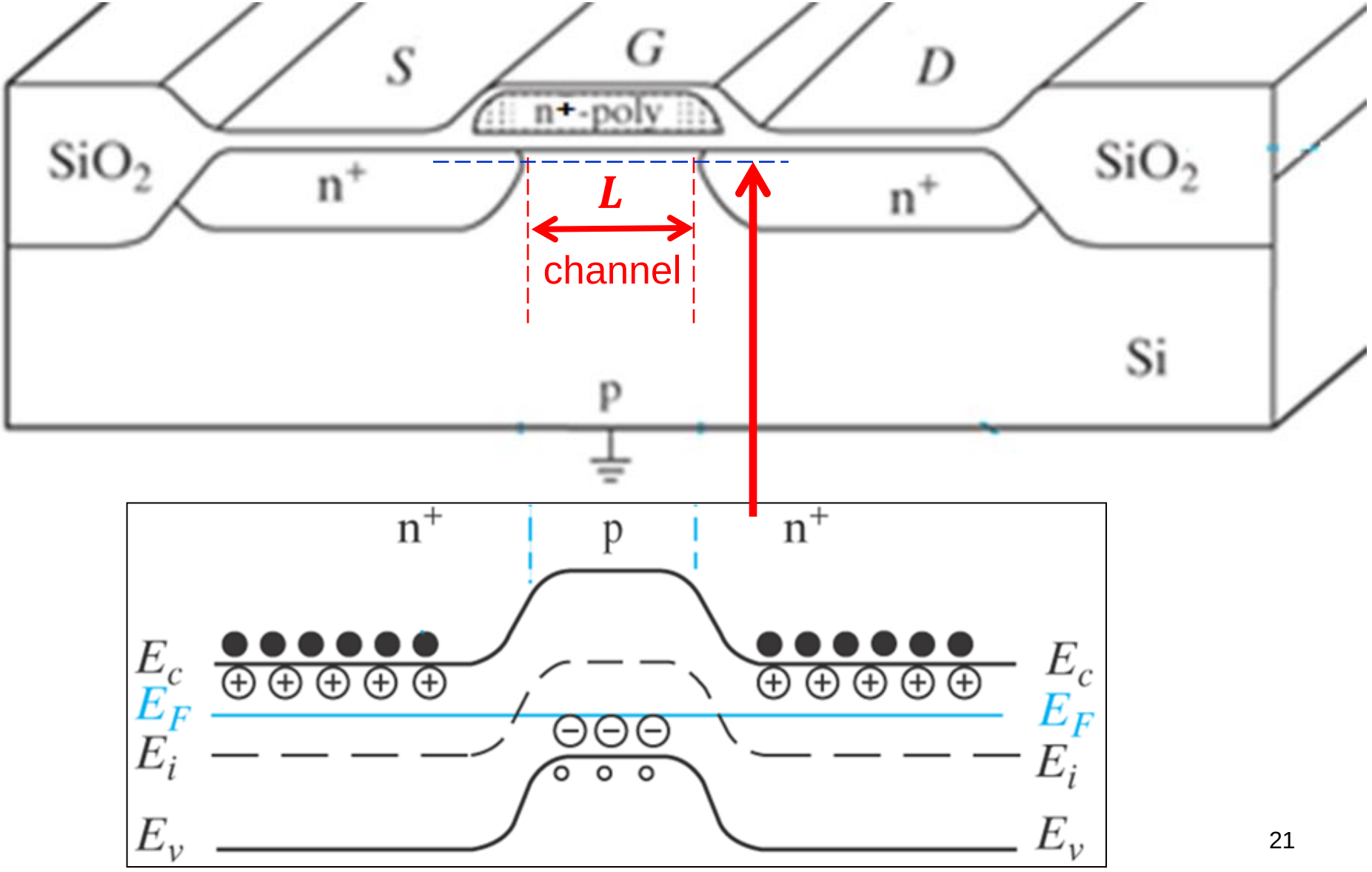
$$= 2.33 \times 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

The MOSFET

When an inversion layer is formed under the gate, current can flow from drain to source (n-channel device)



The MOSFET



MOSFET – Gate Voltage

$$V_G = \underbrace{V_{FB}}_{\text{flat band voltage}} + \underbrace{V_i}_{\text{voltage across oxide}} + \underbrace{\phi_s}_{\text{surface voltage at oxide interface}}$$

$$V_i = \frac{-Q_s d}{\epsilon_i} = \frac{-Q_s}{C_i} = -\frac{Q_n + Q_d}{C_i}$$

per unit area

MOSFET – Gate Voltage

$$V_G = V_{FB} + V_i + \phi_s$$

$$V_G = V_{FB} - \frac{Q_n + Q_d}{C_i} + \phi_s$$

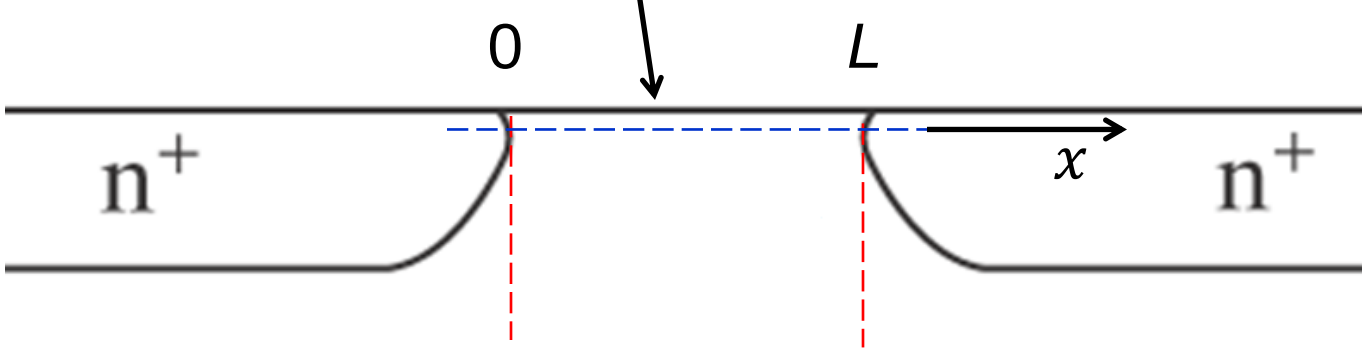
$$\frac{Q_n}{C_i} = -V_G + V_{FB} - \frac{Q_d}{C_i} + \phi_s$$

MOSFET – mobile induced charge Q_n

$$Q_n = -C_i \left[V_G - \underbrace{\left(V_{FB} + \phi_s - \frac{Q_d}{C_i} \right)}_{\text{at threshold this is just } V_T} \right]$$

Now we apply a positive voltage on the drain V_D

$$\phi_s(x) = \underbrace{2\phi_F}_{\text{strong inversion}} + V_x$$



MOSFET – mobile induced charge Q_n

$$Q_n(x) = -C_i\left[V_G - V_{FB} - 2\phi_F - V_x - \frac{Q_d}{C_i}\right]$$

$$W = \sqrt{\frac{2\epsilon_s\phi_s}{qN_A}} \qquad Q_d = -qN_AW = \sqrt{2q\epsilon_S N_A(2\phi_F + V_x)}$$

Now we apply a positive voltage on the drain V_D

$$\phi_s(x) = \underbrace{2\phi_F}_{\text{strong inversion}} + V_x$$

MOSFET – mobile induced charge Q_n

$$Q_n(x) = -C_i\left[V_G - V_{FB} - 2\phi_F - V_x - \frac{Q_d}{C_i}\right]$$

$$V_T$$

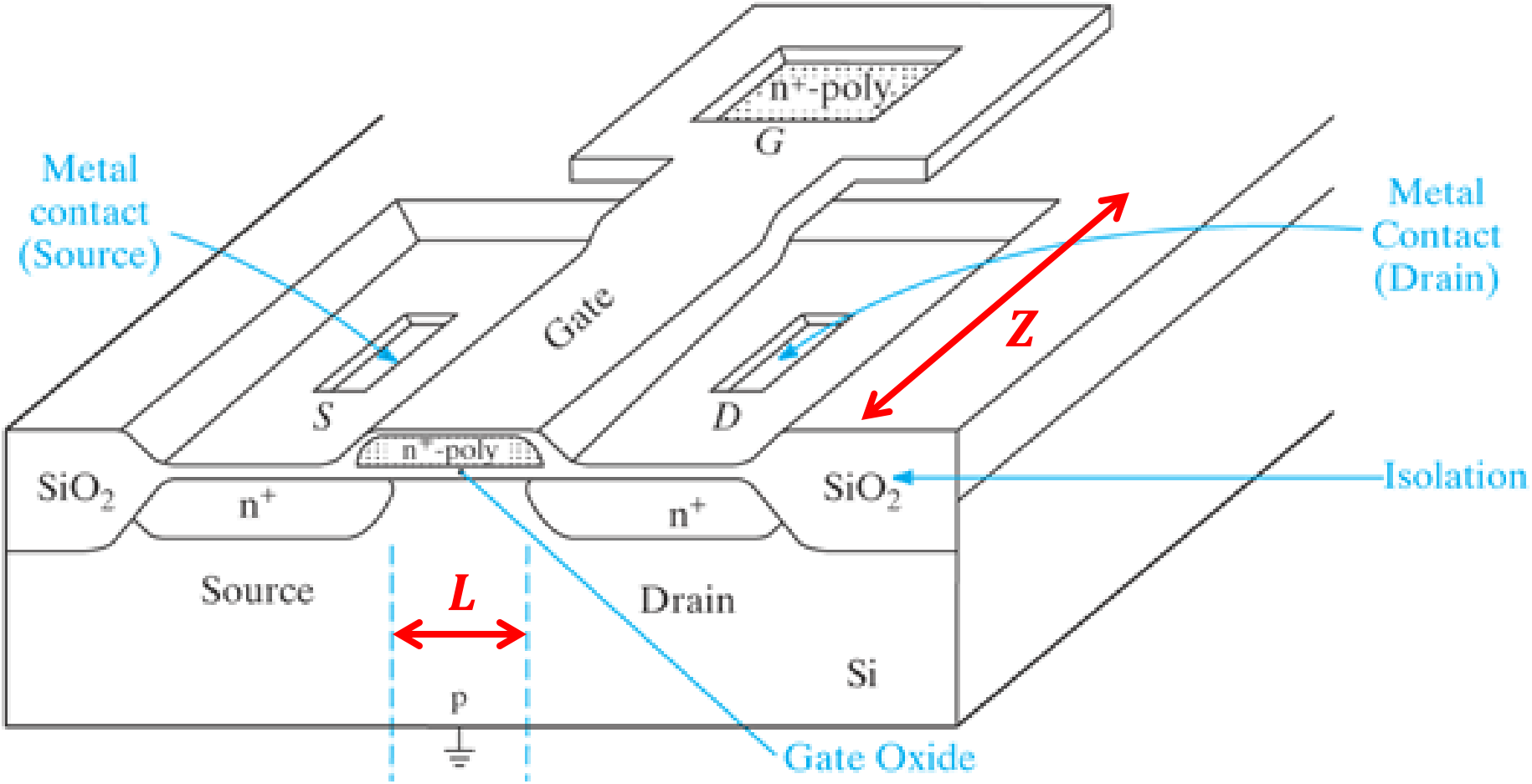
$$Q_d = \sqrt{2q\epsilon_S N_A(2\phi_F + V_x)}$$

If we assume that $Q_d(x)$ does not vary with V_x

$$Q_n(x) = -C_i[V_G - V_T - V_x]$$

mobile charge at any point x in the channel

Remember the width of the channel Z



Current in the channel

$$I_D = \text{Area} \times \text{Charge} \times \text{Velocity}$$

$$I_D = Z \times Q_n \times \underbrace{\overline{\mu_n \mathcal{E}_x}}_{v_{drift}}$$

width of the device

Charge under the gate per unit area of the Si/SiO_2 interface

channel conductance at x

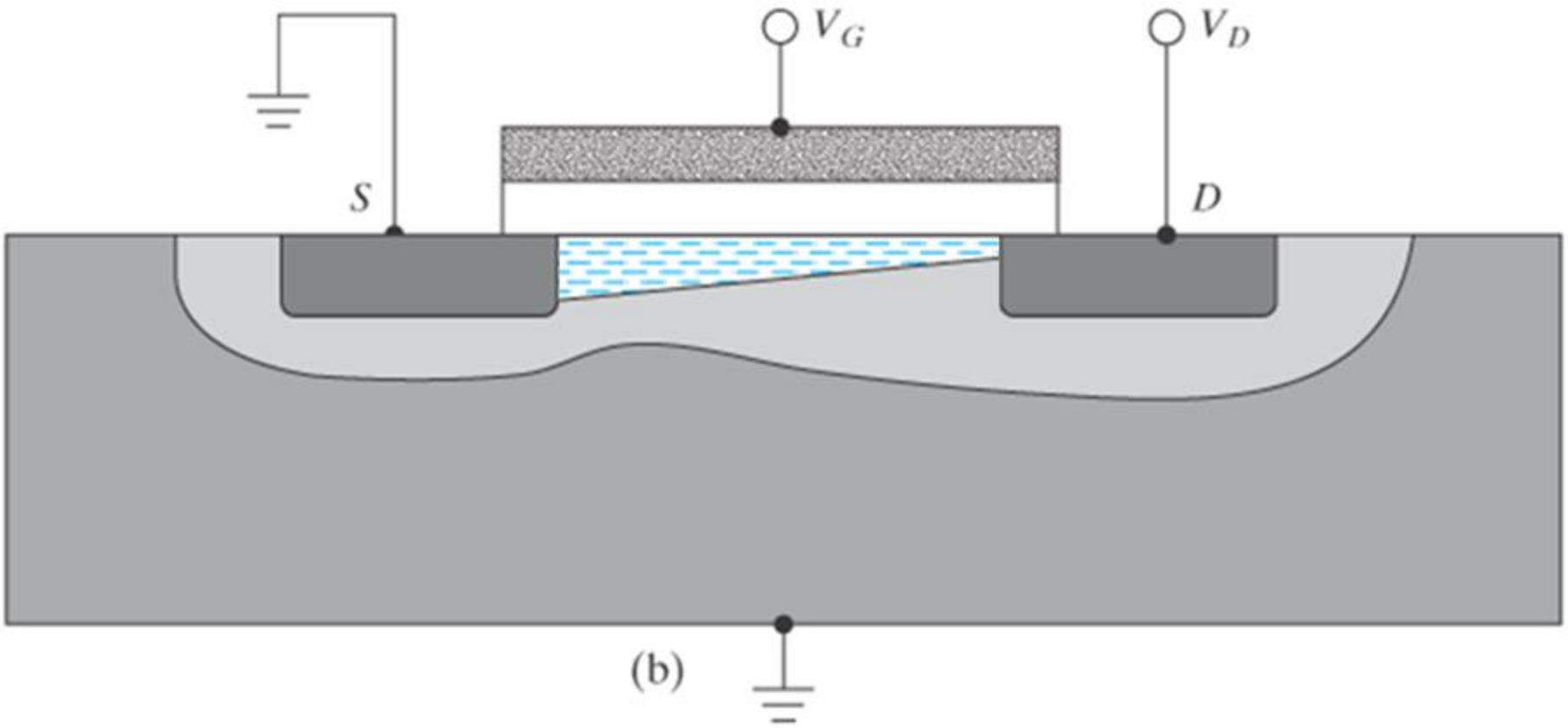
$$I_D = \underbrace{\frac{\overline{\mu_n}\,|Q_n(x)|\,Z}{dx}}_{g(x)} dV_x$$

$\overline{\mu_n}$ surface electron mobility

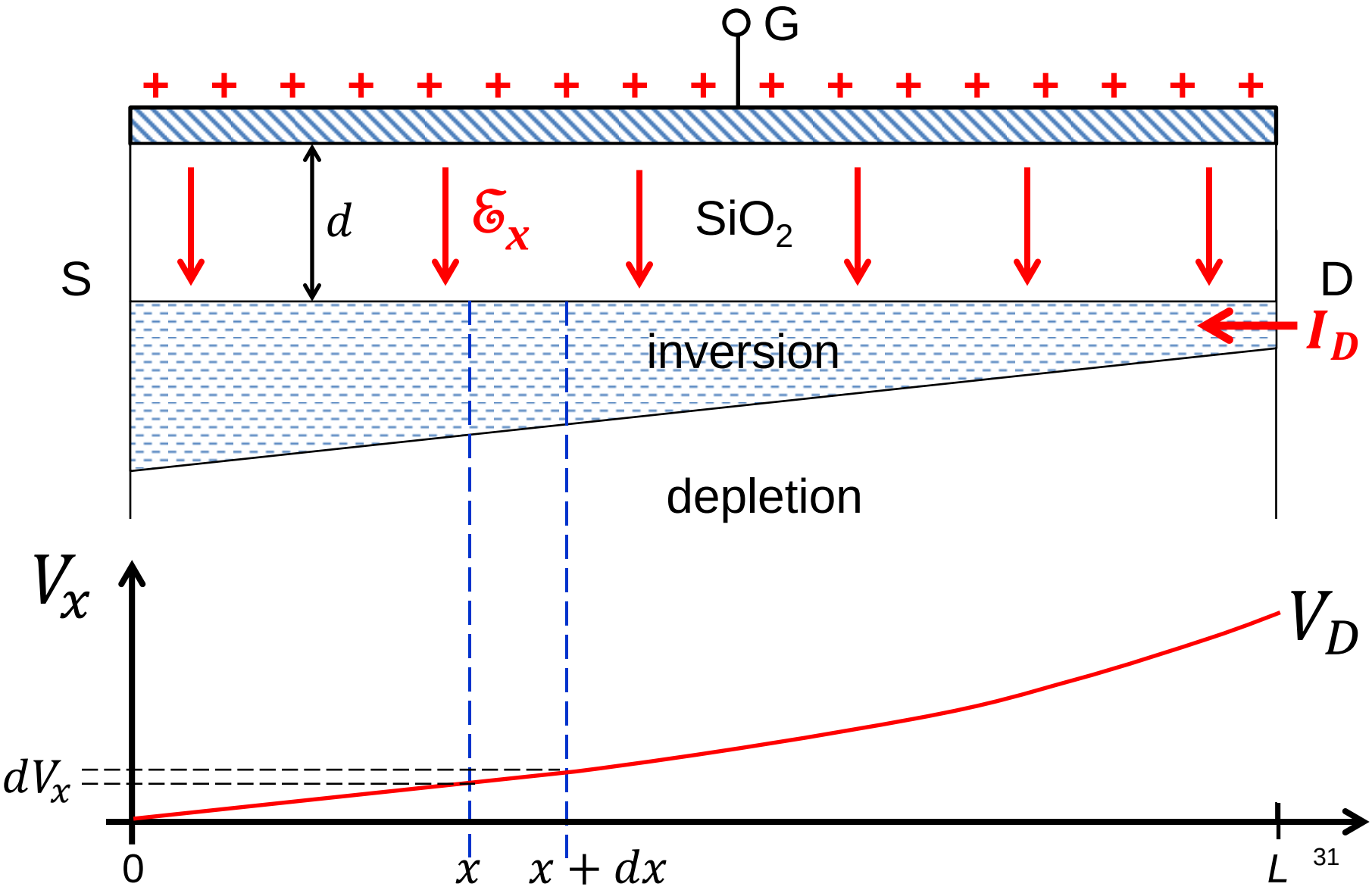
mobility in the narrow layer close to the surface is much lower than in the free bulk due to surface roughness irregularities and quantum effects

Z width of the channel

MOSFET – channel current at x



MOSFET – channel current at x



MOSFET – Drain Current

$$I_D dx = \overline{\mu_n}\, Z\, |Q_n(x)|\, dV_x$$

$$Q_n(x) = -C_i[V_G - V_T - V_x]$$

$$\int_0^L I_D\, dx = \overline{\mu_n} Z C_i \int_0^{V_D} (V_G - V_T - V_x)\; dV_x$$

$$I_D = \underbrace{\frac{\overline{\mu_n} Z C_i}{L}}_{k_N}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

MOSFET – Drain Current

$$I_D = k_N \left[(V_G - V_T) V_D - \frac{1}{2} V_D^2 \right]$$

Reasonable approximation at low drain voltage but with the assumption Q_D independent of V_D. More general result:

$$I_D = k_N \left[\left(V_G - V_{FB} - 2\phi_F - \frac{1}{2} V_D \right) V_D - \frac{2}{3} \frac{\sqrt{2\epsilon_s q N_A}}{C_i} \left\{ (V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2} \right\} \right]$$

MOSFET – Conductance of channel

linear region

$$I_D = \frac{\overline{\mu_n} Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

$V_D \ll (V_G - V_T)$ (linear region)
$V_G > V_T$ (channel condition)

$$g = \frac{\partial I_D}{\partial V_D} = \frac{\overline{\mu_n} Z C_i}{L}(V_G - V_T)$$
$$= k_N(\text{lin.})\,(V_G - V_T)$$

MOSFET – Saturation

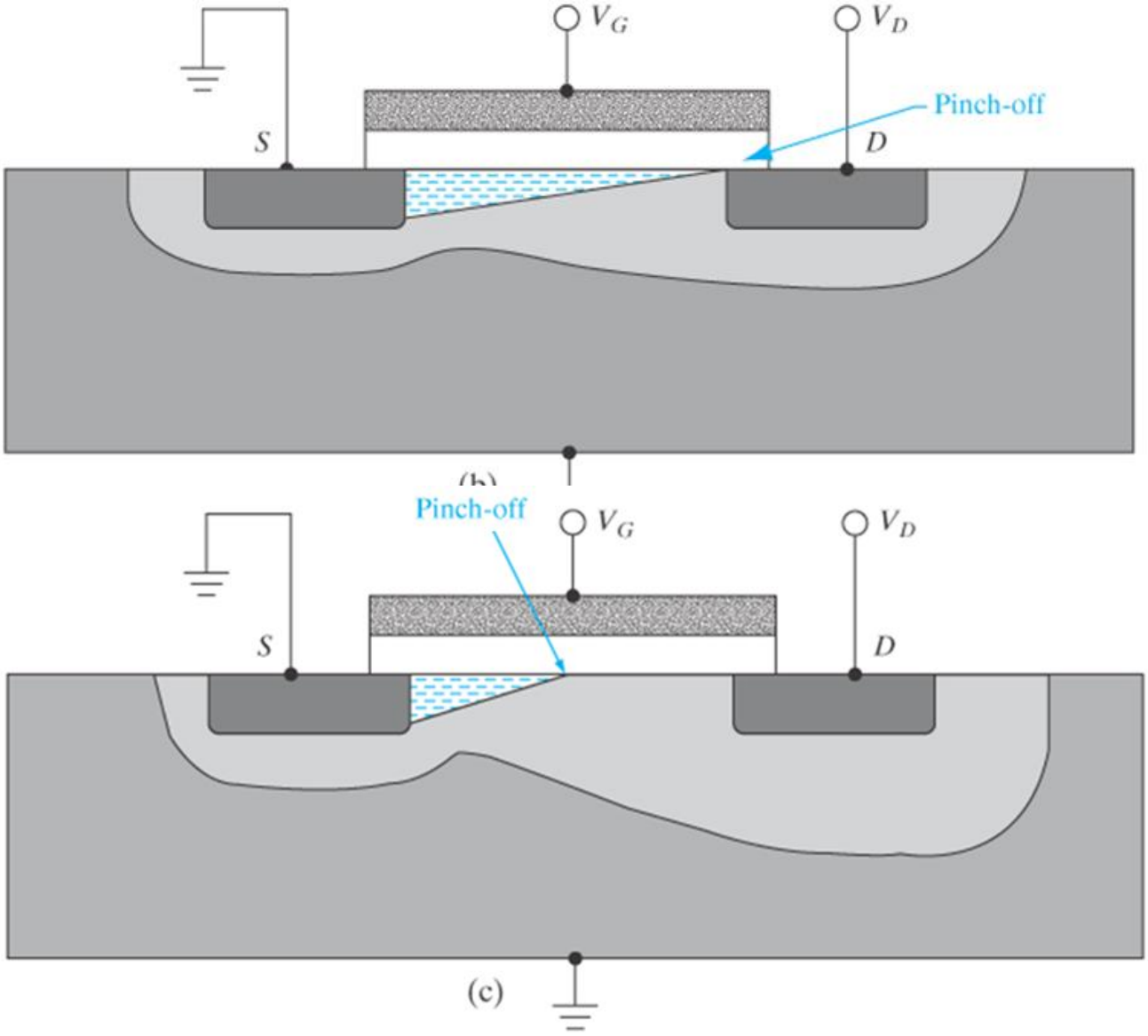
As the drain voltage is increased, the voltage across the oxide decreases near the drain as does Q_S.

The channel goes into “pinch off” at the drain and current saturates

in saturation condition we have approximately

$$V_D(\text{sat.}) \approx (V_G - V_T)$$

MOSFET – Saturation



onset of saturation

deep saturation

MOSFET – Transconductance

saturation region $\boxed{V_D(\text{sat.}) \approx (V_G - V_T)}$

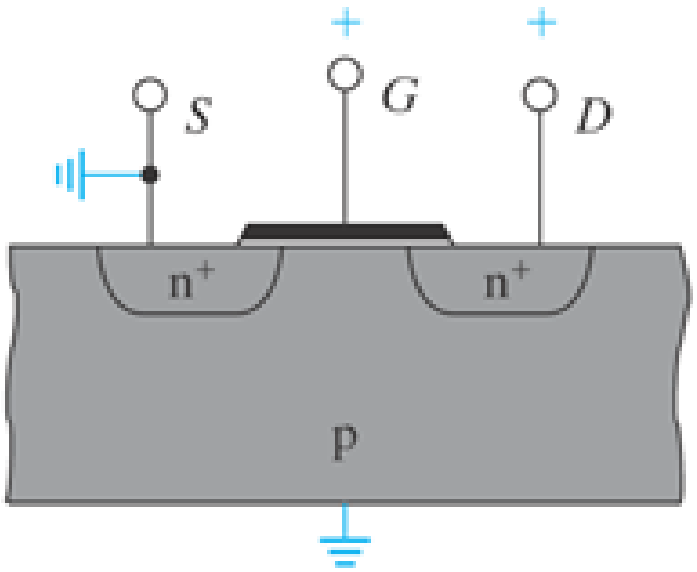
$$I_D(\text{sat.}) = \frac{\overline{\mu_n} Z C_i}{2L}(V_G - V_T)^2$$

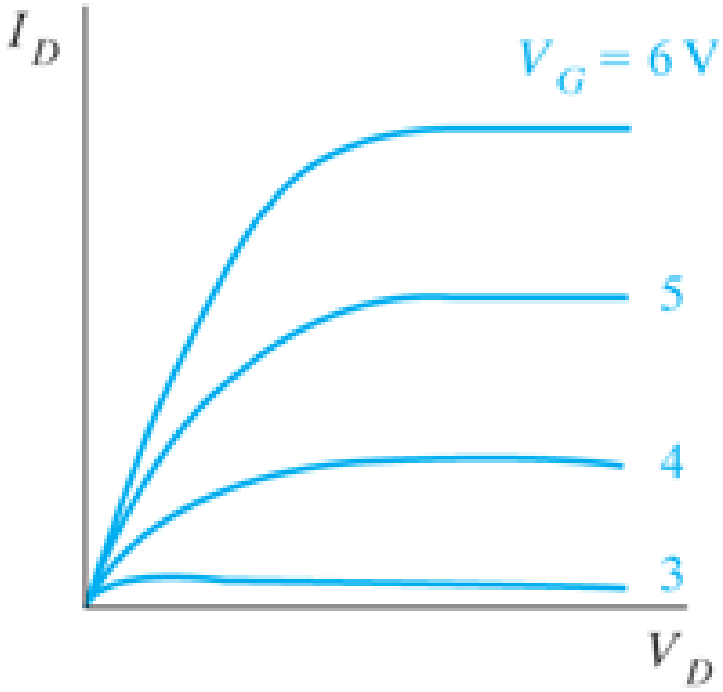
$$= \frac{Z}{2L}\overline{\mu_n}\ C_i\ V_D^2(\text{sat.}) = \frac{k_N(\text{sat})}{2} V_D^2(\text{sat.})$$

transconductance in saturation region

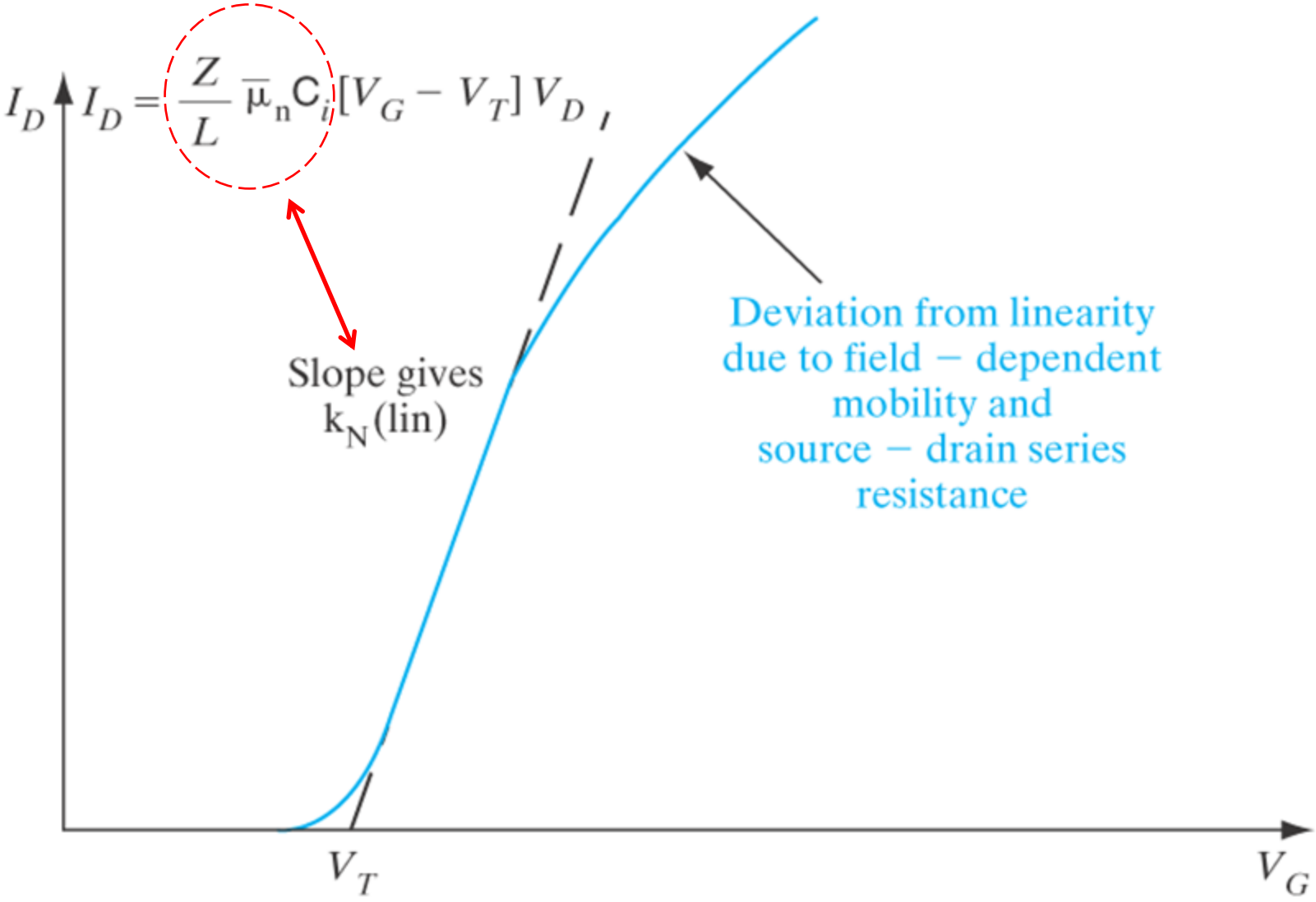
$$g_m = \frac{\partial I_D(\text{sat.})}{\partial V_G} = \frac{\overline{\mu_n} Z C_i}{L}(V_G - V_T)$$

MOSFET – Transconductance



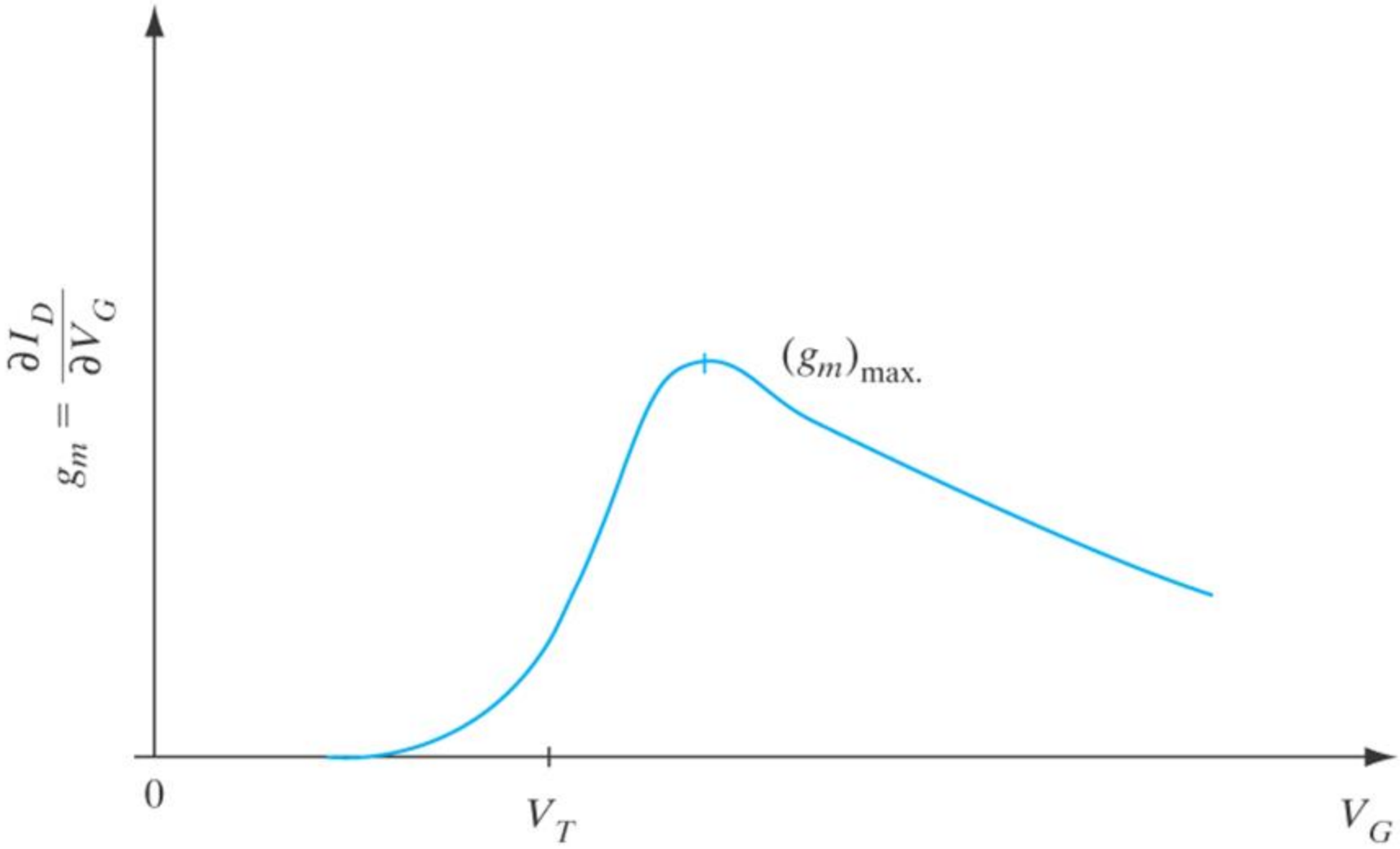


MOSFET – Transfer characteristics

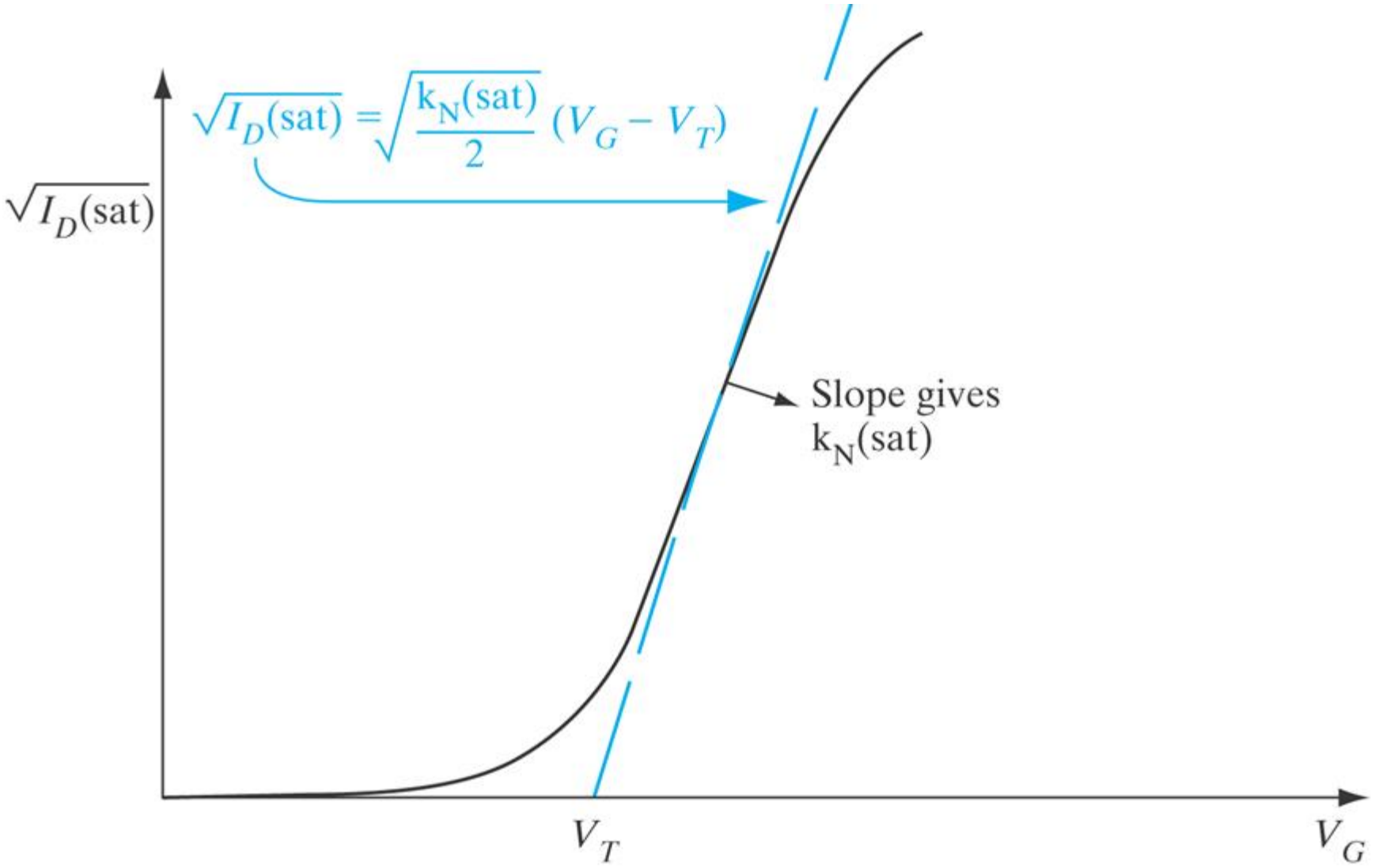


MOSFET – Transfer characteristics

transconductance



MOSFET – Transfer characteristics



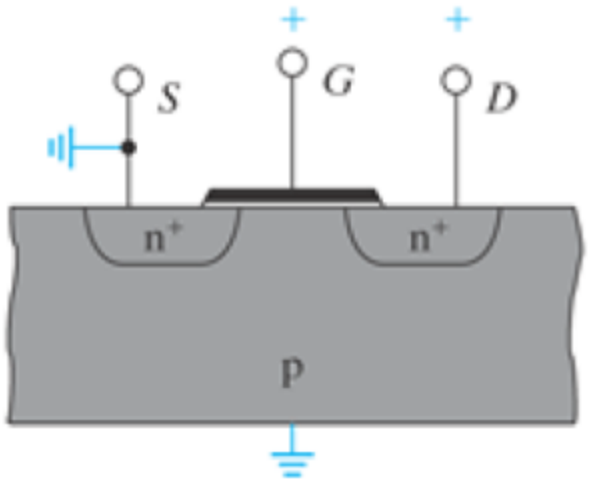
ECE 340 Lecture 36
Semiconductor Electronics

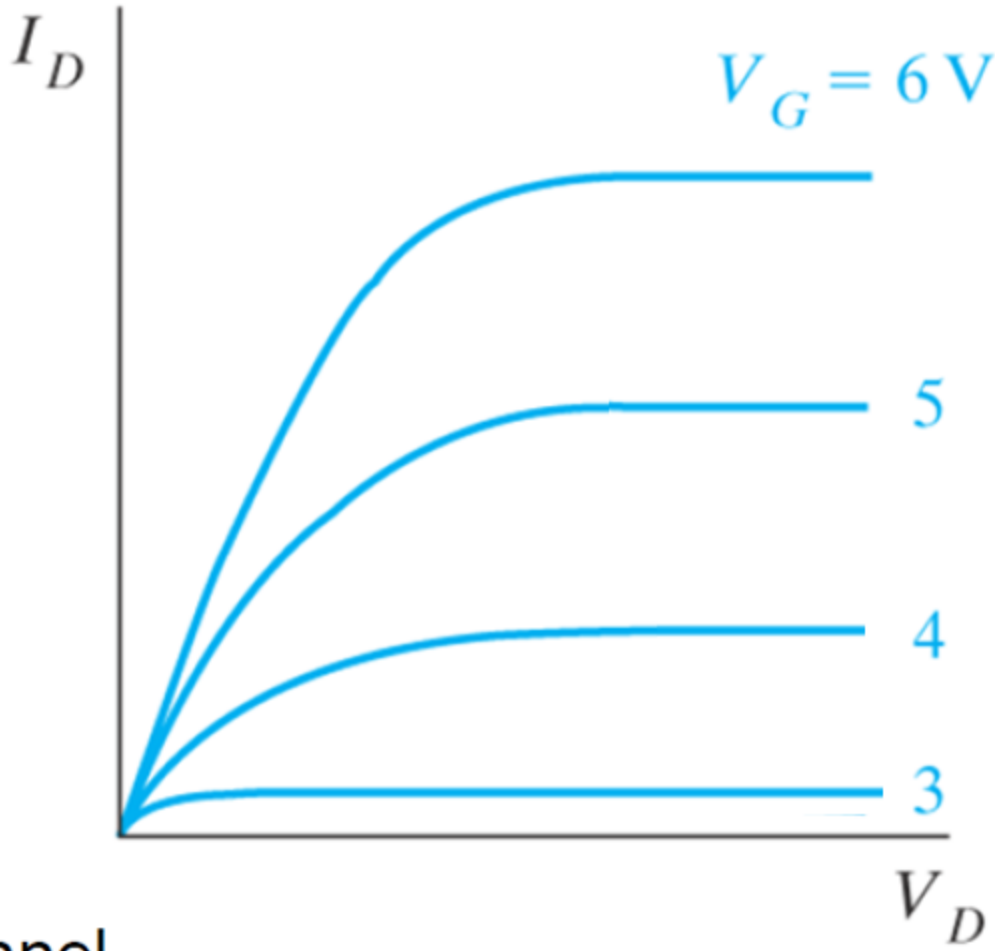
Spring 2022
10:00-10:50am
Professor Umberto Ravaioli
Department of Electrical and Computer Engineering
2062 ECE Building

Today's Discussion

- **Equivalent circuit for the MOSFET**
- **CMOS integration**
- **Logic devices**

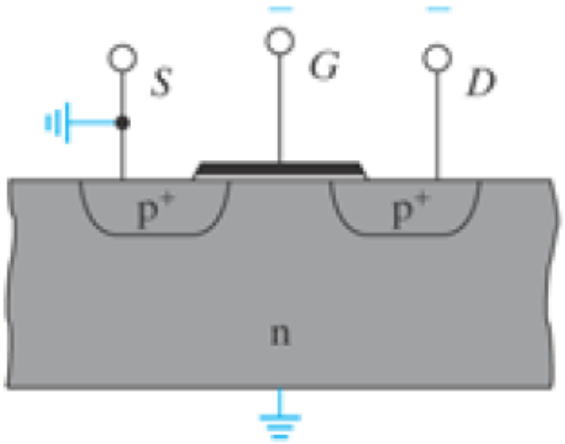
I-V Curves

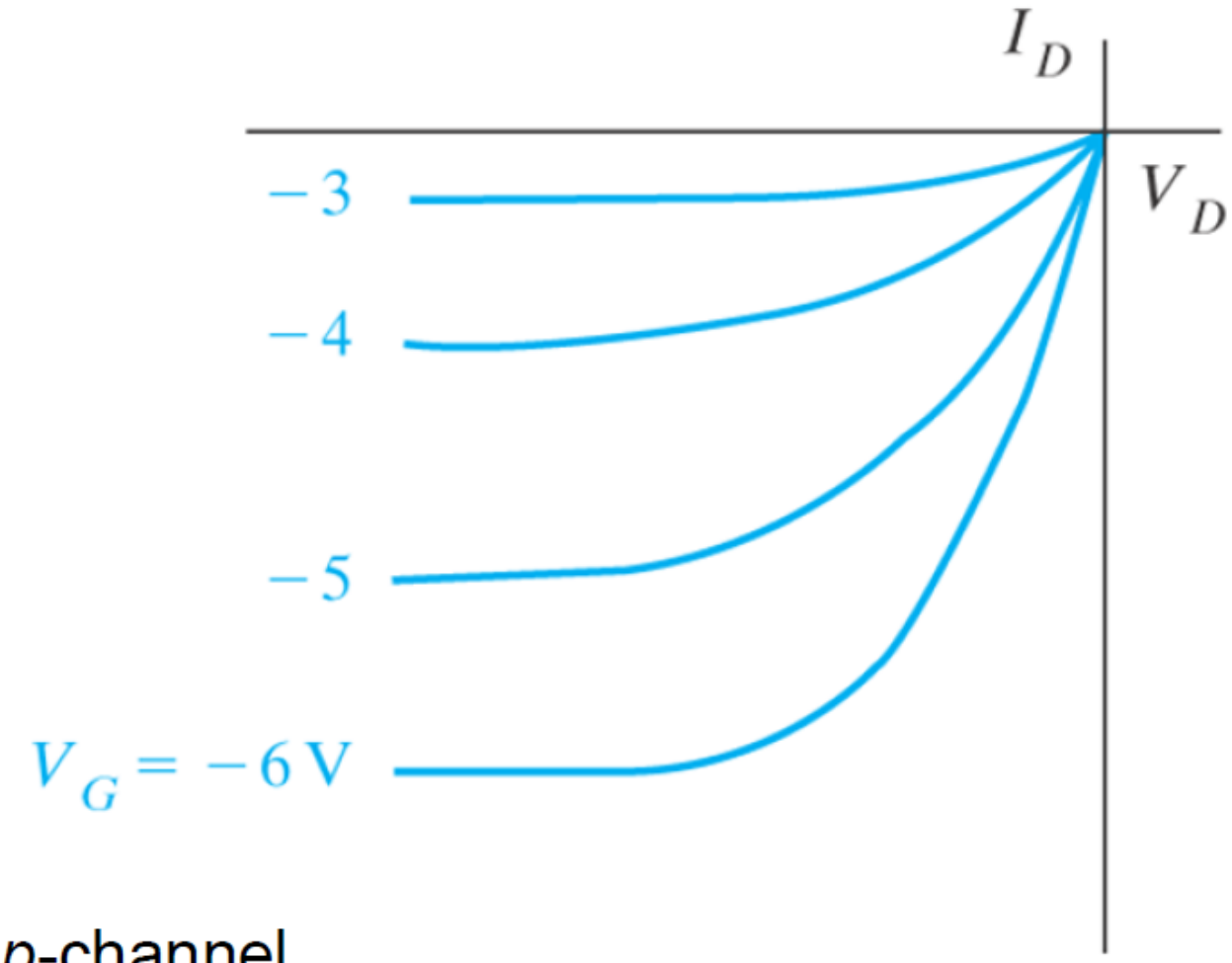




n-channel

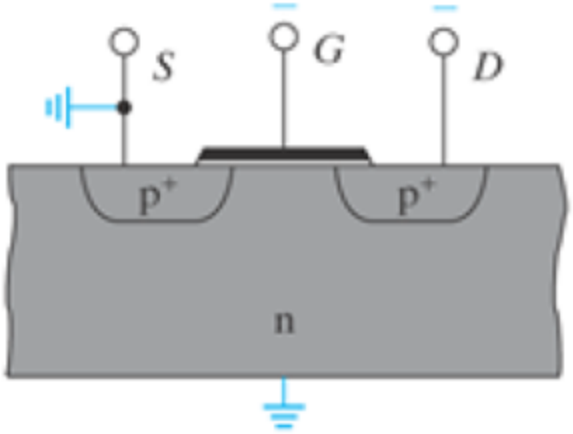
I-V Curves



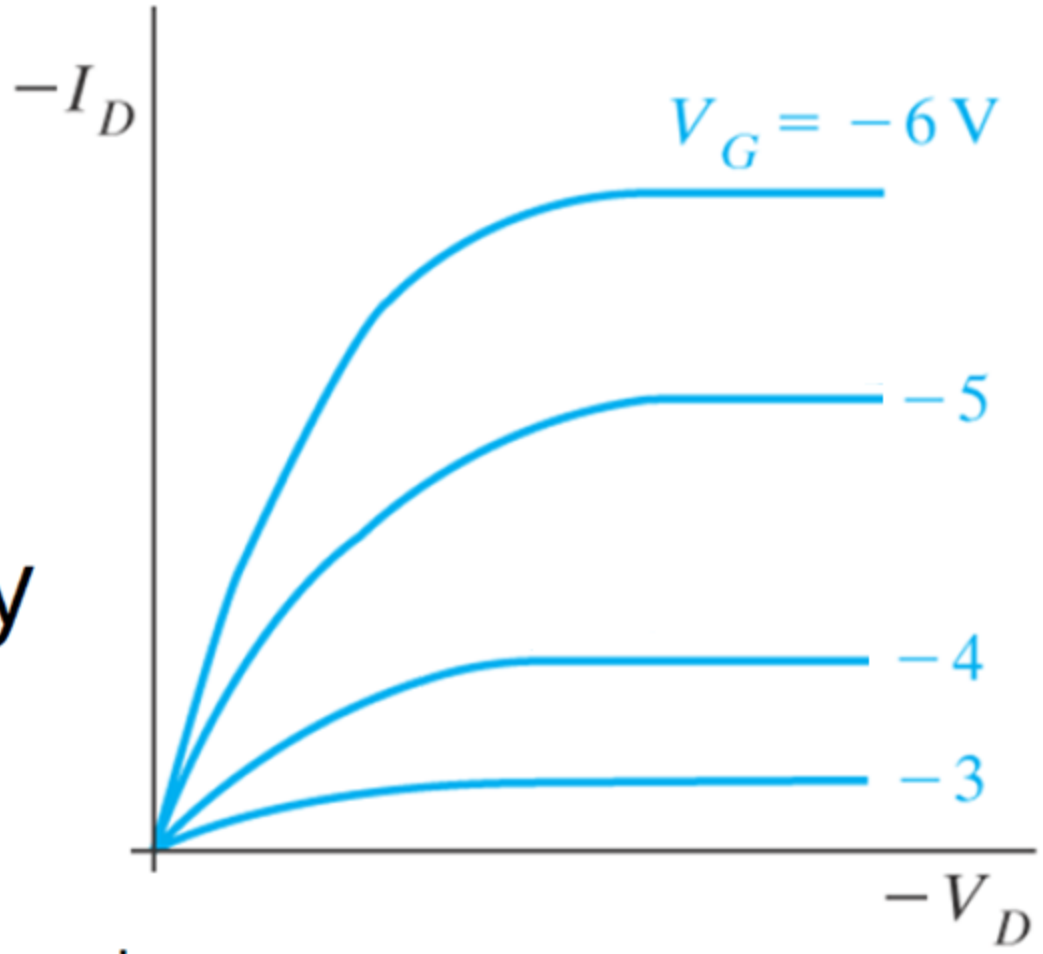


p-channel

I-V Curves



or equivalently



p-channel

MOSFET – Example

n-channel MOSFET

$d = 10\ \text{nm} = 10^{-6}\ \text{cm}$

$V_T = 0.6\text{V}$

$Z = 25\mu\text{m}$

$L = 1\ \mu\text{m}$

$\overline{\mu_n} = 200\ \text{cm}^2/\text{V}\cdot\text{s}$

$$C_i = \frac{\epsilon_i}{d} = \frac{3.9 \times 8.85 \times 10^{-14}}{10^{-6}}$$

$$= 3.45 \times 10^{-7}\ \text{F/cm}^2 \text{ (unit area)}$$

$$k_N = \frac{\overline{\mu_n} Z C_i}{L} = \frac{200 \times 25 \times 10^{-4} \times 3.45 \times 10^{-7}}{10^{-4}} = .001725$$

$V_G = 5\ \text{V}$ $V_D = 0.1\ \text{V}$ $V_D = 0.1\ \text{V} < (V_G - V_T) = 4.4\ \text{V}$

linear region

$$I_D = \frac{\overline{\mu_n} Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] =$$

$$= \underbrace{0.001725 \times ((5 - 0.6) \times 0.1}_{7.59 \times 10^{-4}} - 0.5 \times 0.1^2) = 7.5 \times 10^{-4}\text{A}$$

MOSFET – Example

n-channel MOSFET

$d = 10\ \text{nm} = 10^{-6}\ \text{cm}$

$V_T = 0.6\text{V}$

$Z = 25\mu\text{m}$

$L = 1\ \mu\text{m}$

$\overline{\mu_n} = 200\ \text{cm}^2/\text{V}\cdot\text{s}$

$V_G = 3\ \text{V}$ $V_D = 5\ \text{V}$

$V_D = 5\ \text{V} > (V_G - V_T) = 2.4\ \text{V}$

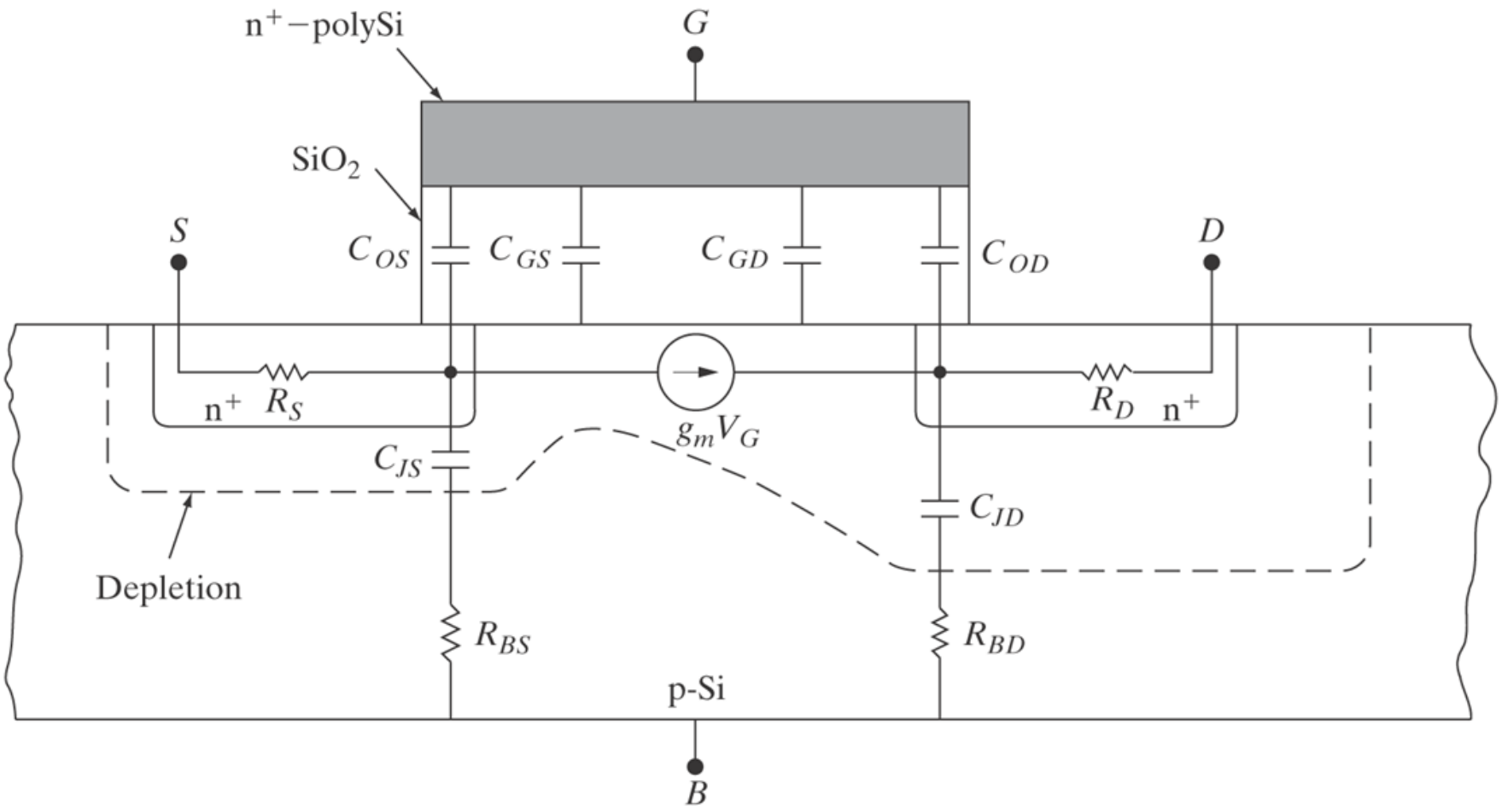
$V_D(\text{sat.}) = 2.4\ \text{V}$ saturation region

$$k_N = \frac{\overline{\mu_n} Z C_i}{L} = .001725$$

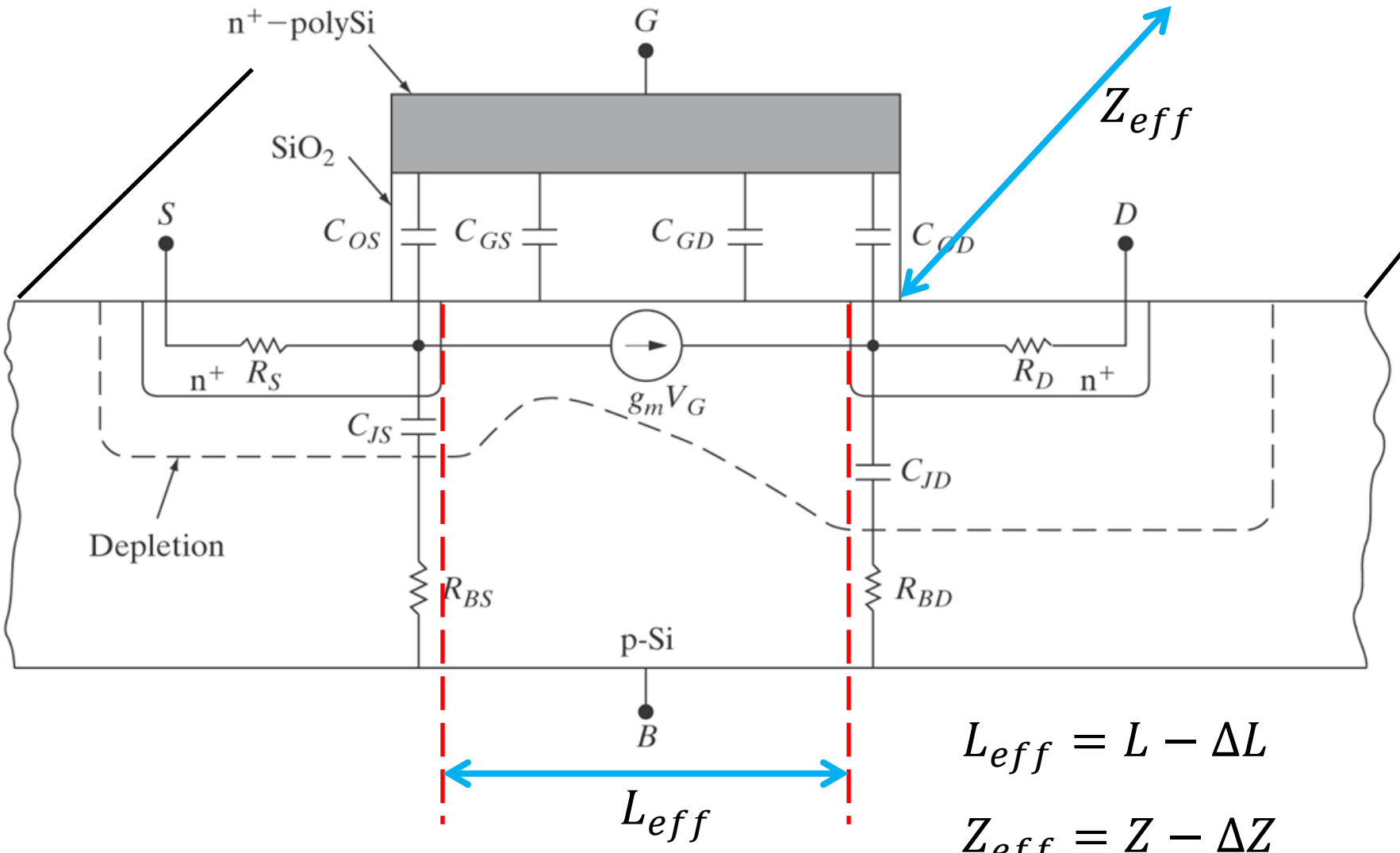
$$I_D = \frac{\overline{\mu_n} Z C_i}{L}\left[(V_G - V_T)V_D(\text{sat.}) - \frac{1}{2}V_D^2(\text{sat.})\right] =$$
$$= 0.001725 \times ((3 - 0.6) \times 2.4 - 0.5 \times 2.4^2)$$
$$= 4.968 \times 10^{-3}\text{A}$$

$V_D = 7\ \text{V} > (V_G - V_T) \rightarrow V_D(\text{sat.}) = 2.4\ \text{V} \rightarrow I_D$ is the same

MOSFET equivalent circuit



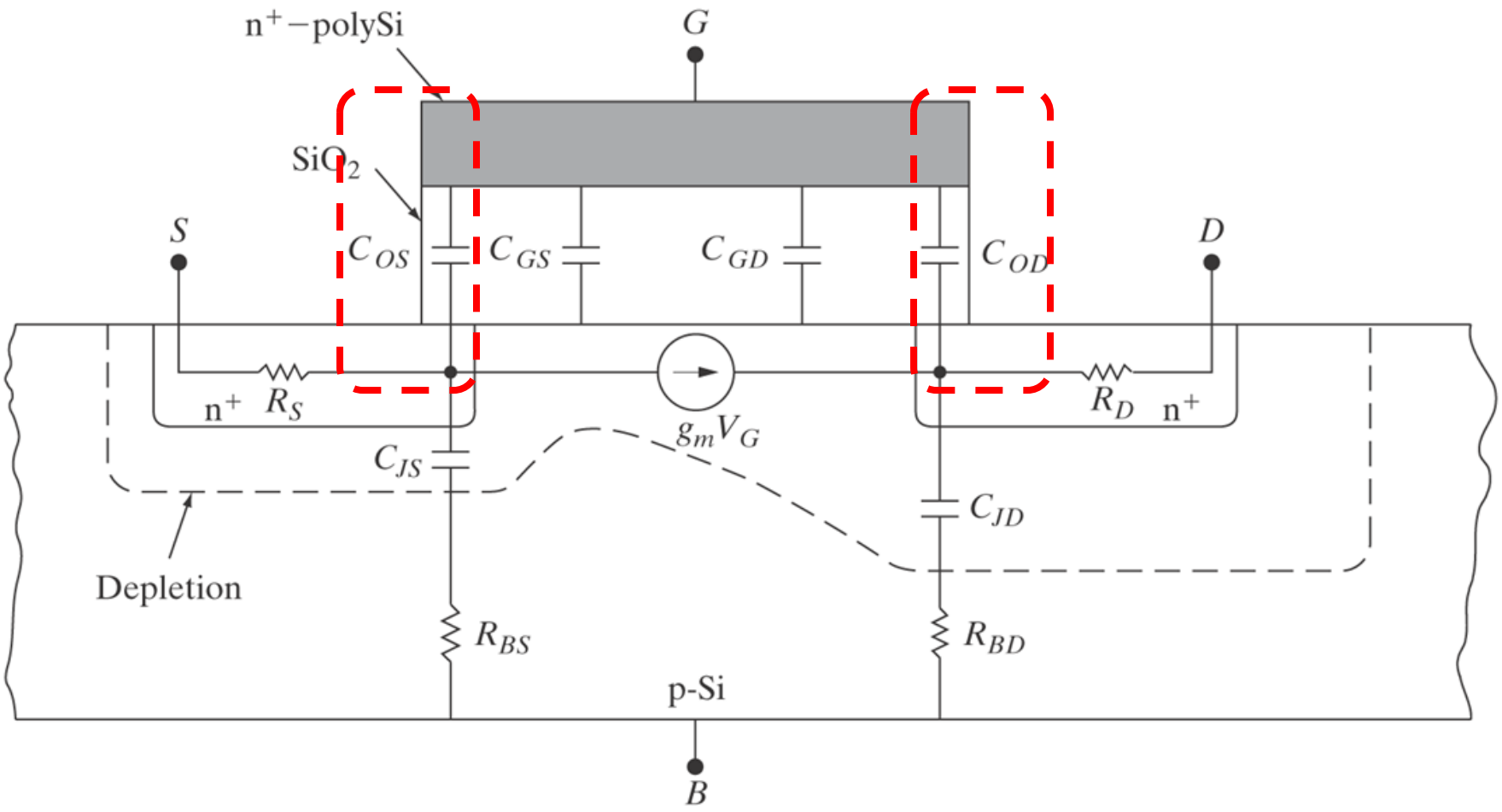
MOSFET equivalent circuit



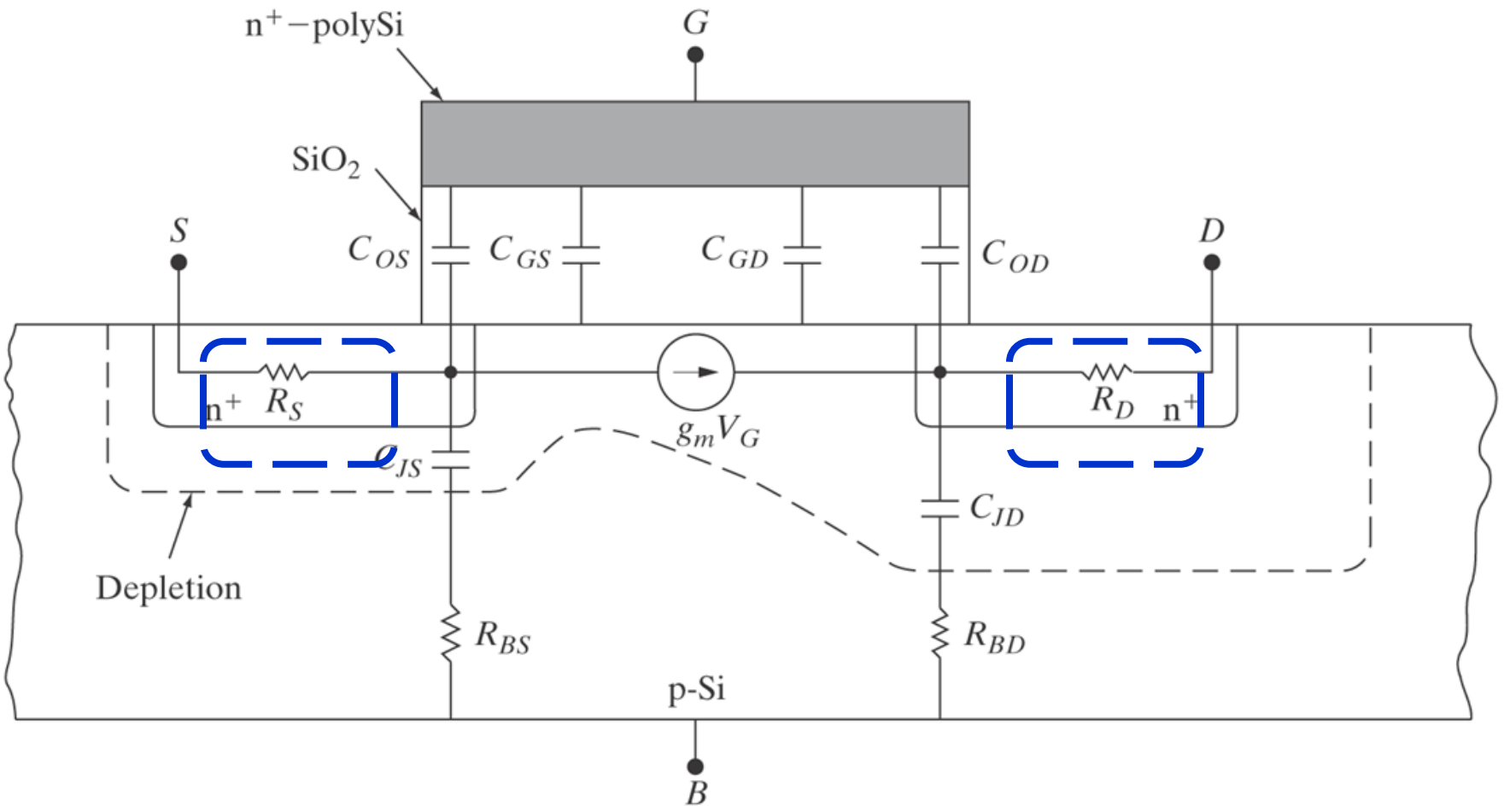
$$L_{eff} = L - \Delta L$$

$$Z_{eff} = Z - \Delta Z$$

MOSFET equivalent circuit

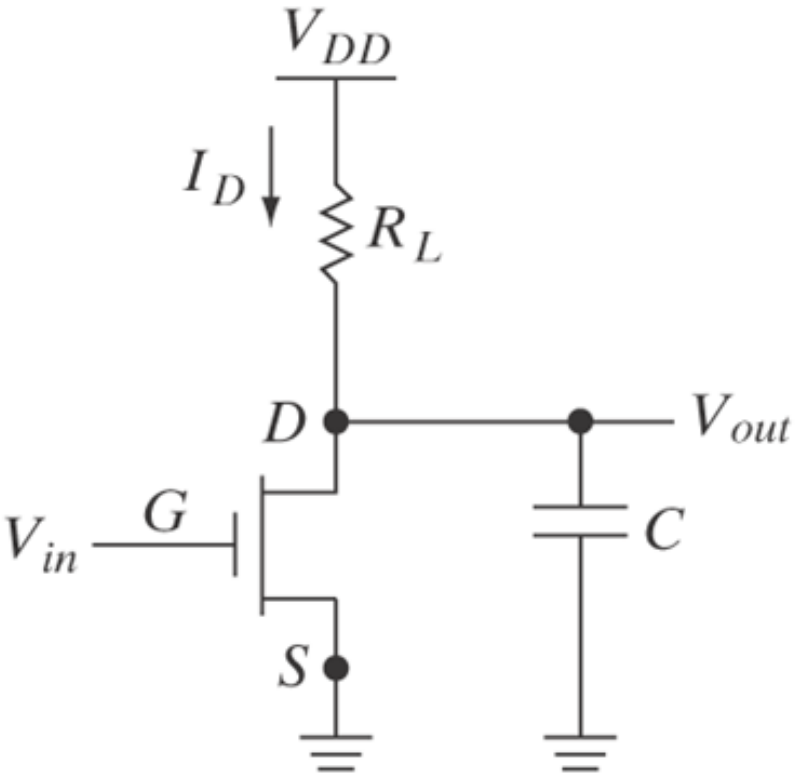


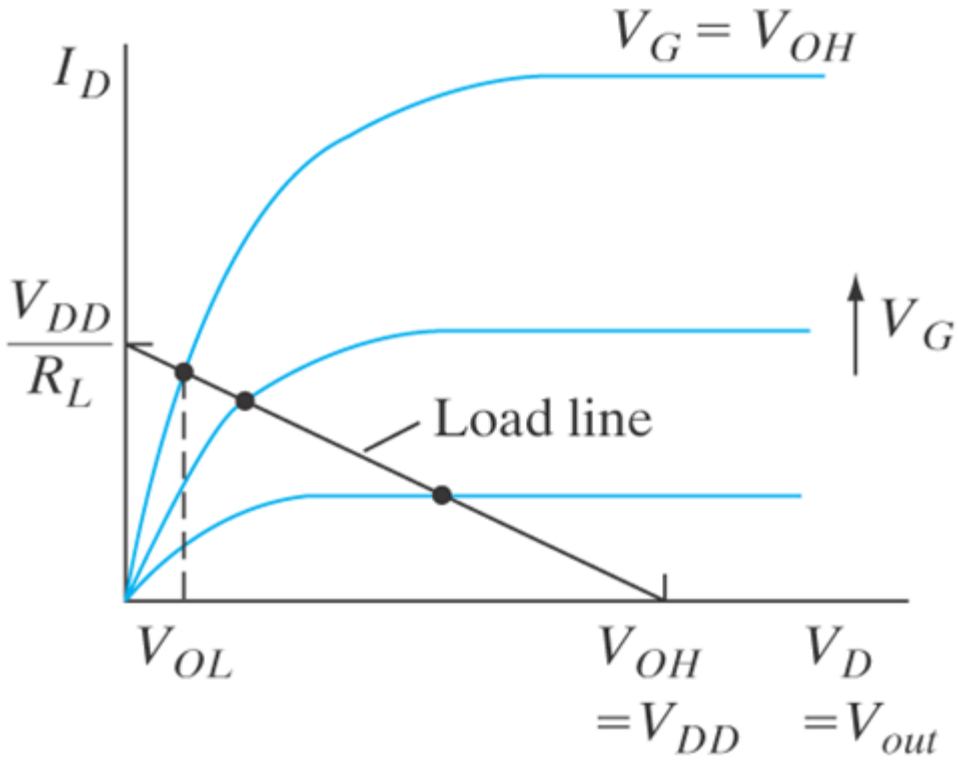
MOSFET equivalent circuit



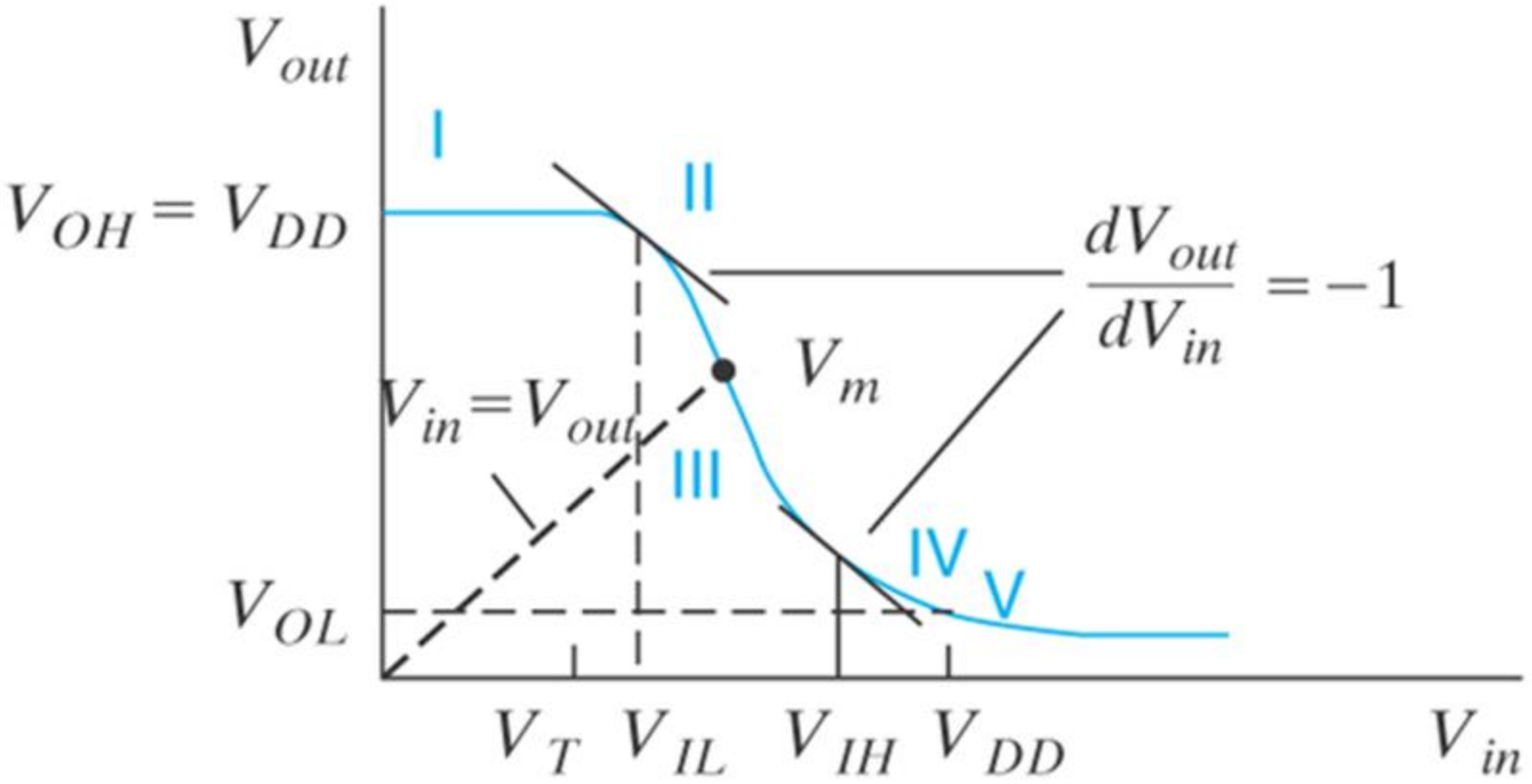
$$\frac{V_D}{I_D} = R_{Ch} + R_{SD} = \frac{L - \Delta L}{Z - \Delta Z} \frac{1}{\bar{\mu}_n C_i \left(V_G - V_T \right)} + R_{SD}$$

MOS inverter

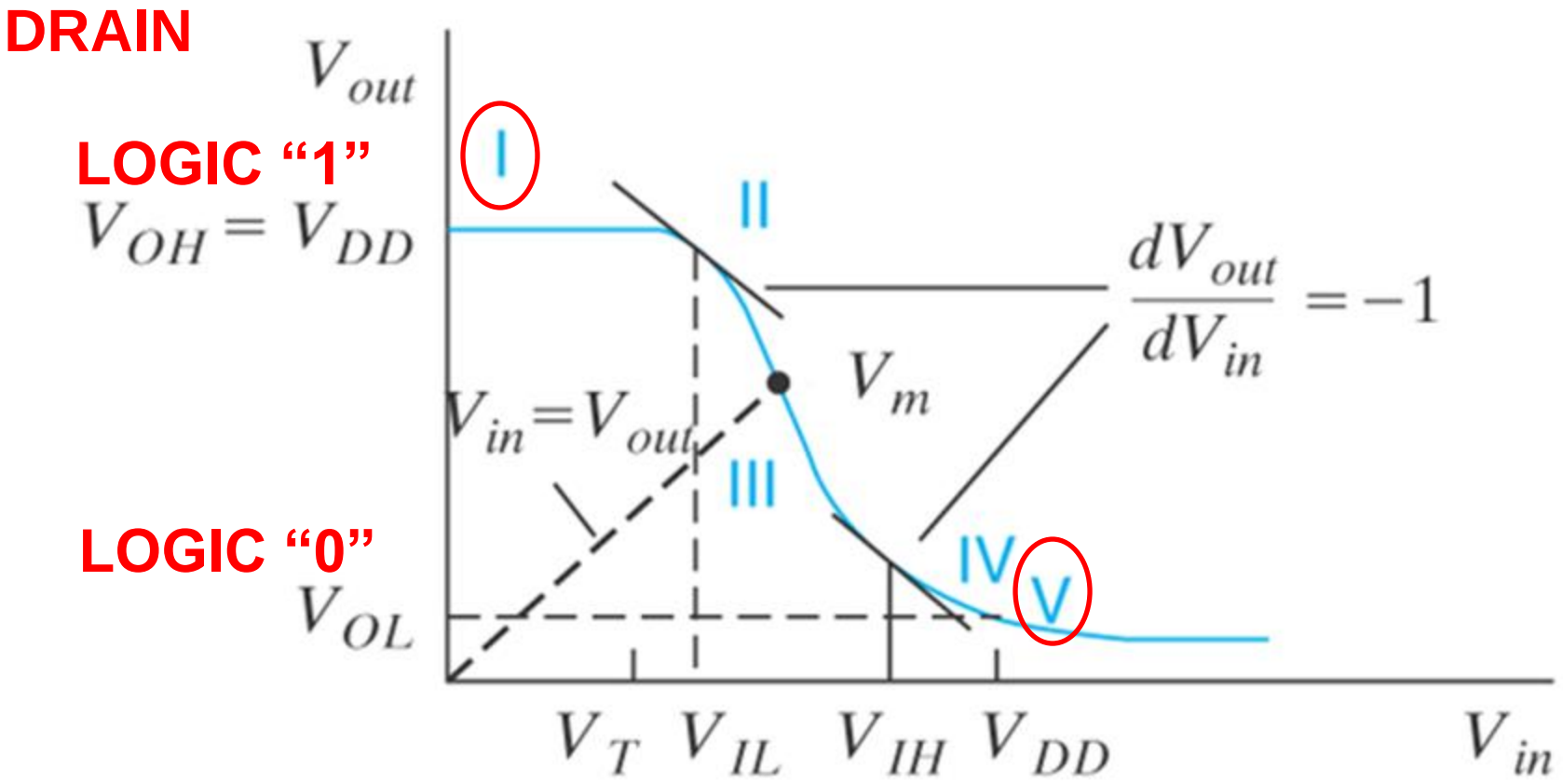




MOS inverter – Voltage transfer characteristics (VTC)

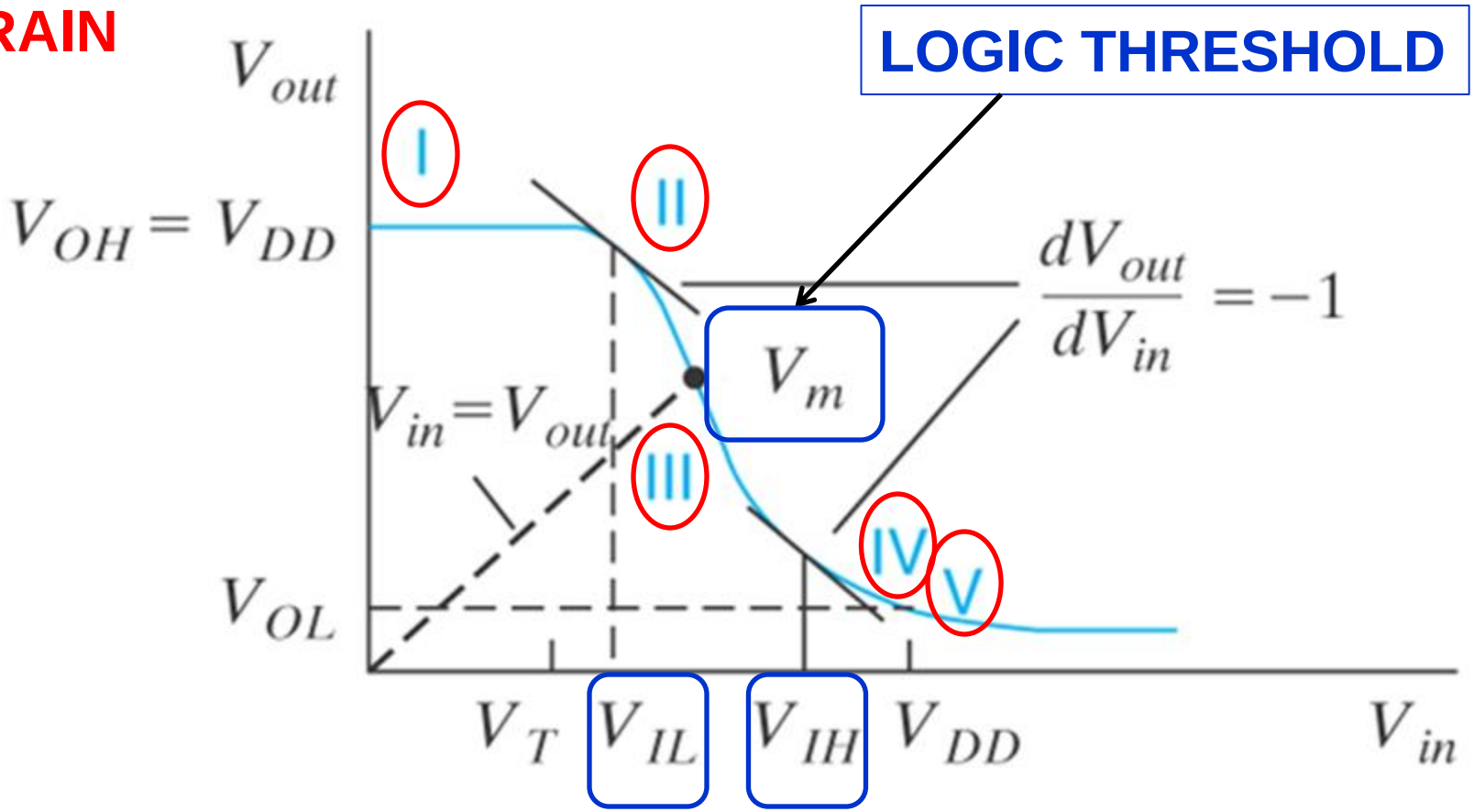


MOS inverter – Voltage transfer characteristics (VTC)



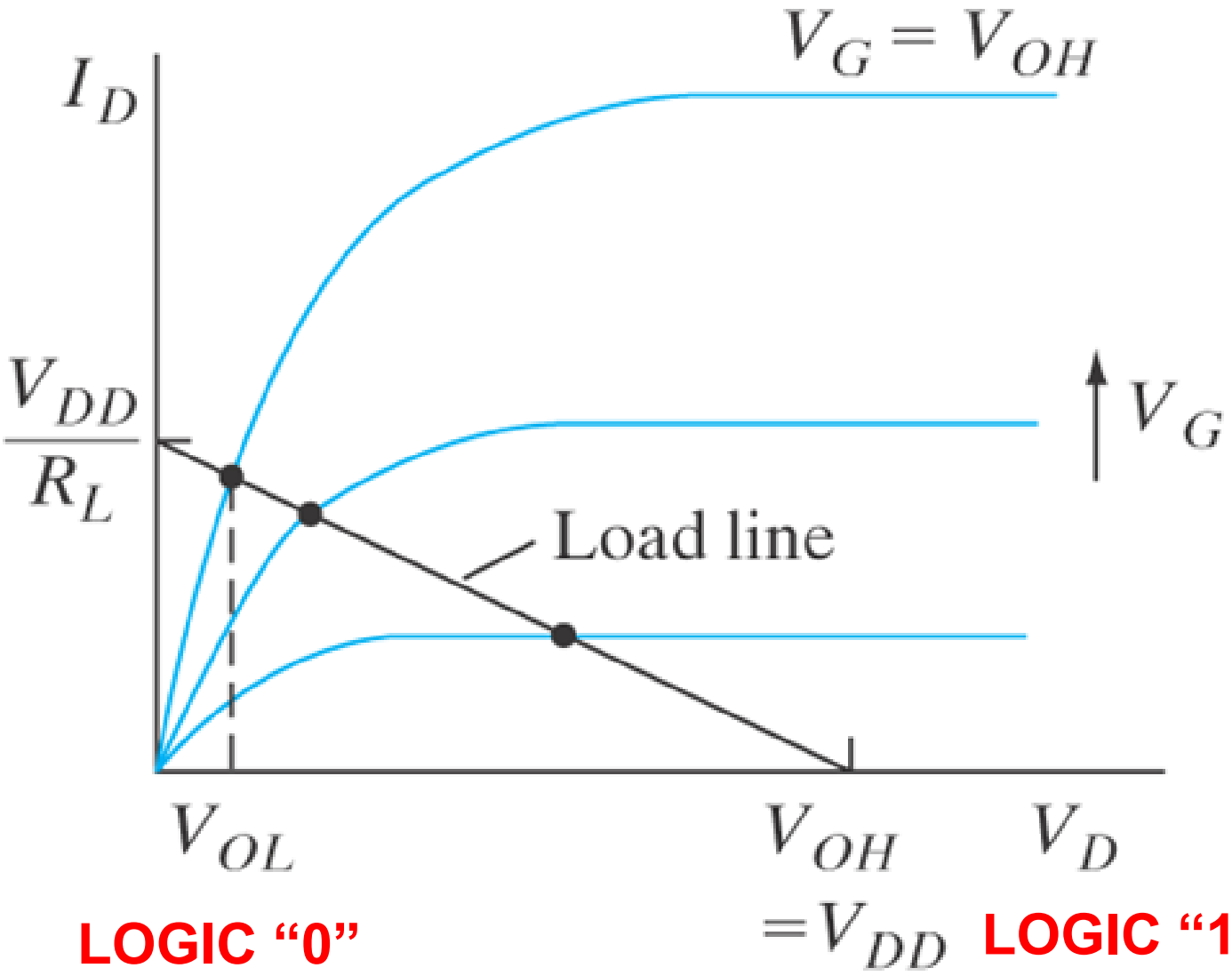
MOS inverter – Voltage transfer characteristics

DRAIN



GATE

MOS inverter – Voltage transfer characteristics



MOS inverter – Example: Determine V_{OL}

MOSFET Drain Current (linear region):

$$I_D = k\left[V_G - V_T - \frac{V_D}{2}\right]V_D = k\left[V_{DD} - V_T - \frac{V_{OL}}{2}\right]V_{OL}$$

Resistor Current (equal to MOSFET current):

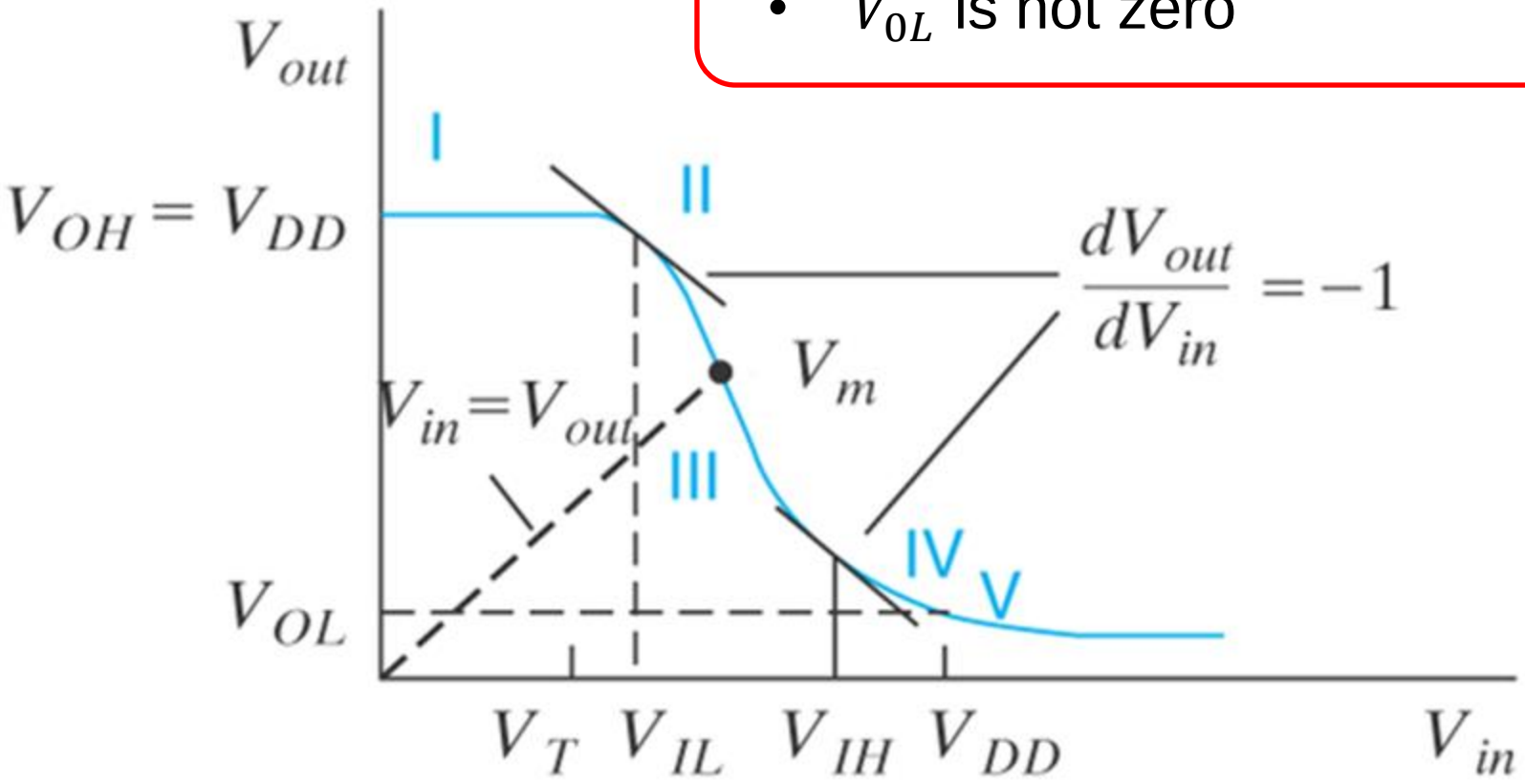
$$I_R = I_D = \frac{V_{DD} - V_{OL}}{R_L}$$

MOSFET Drain Current (saturation region):

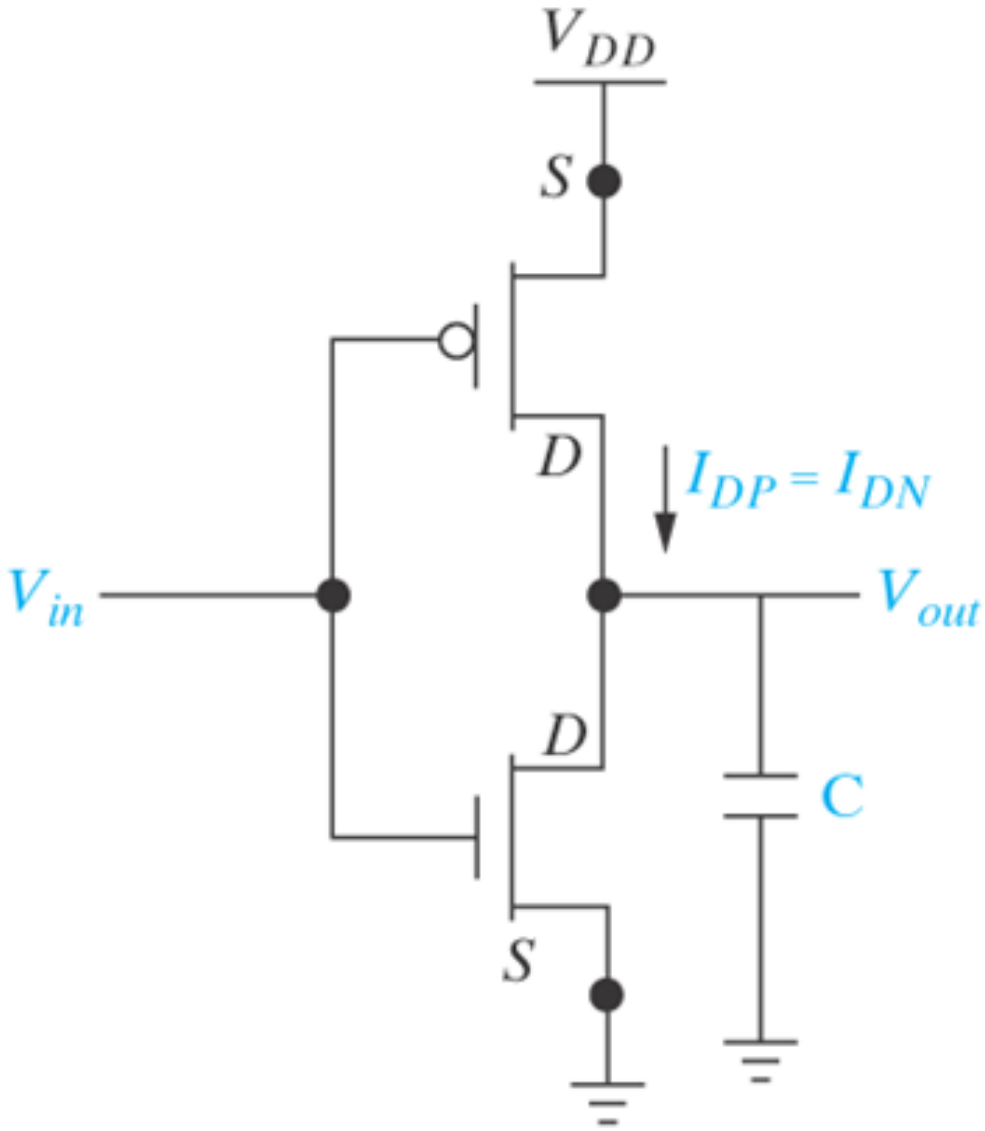
$$I_D = \frac{1}{2}k\left[V_G - V_T\right]^2$$

MOS inverter – Voltage transfer characteristics

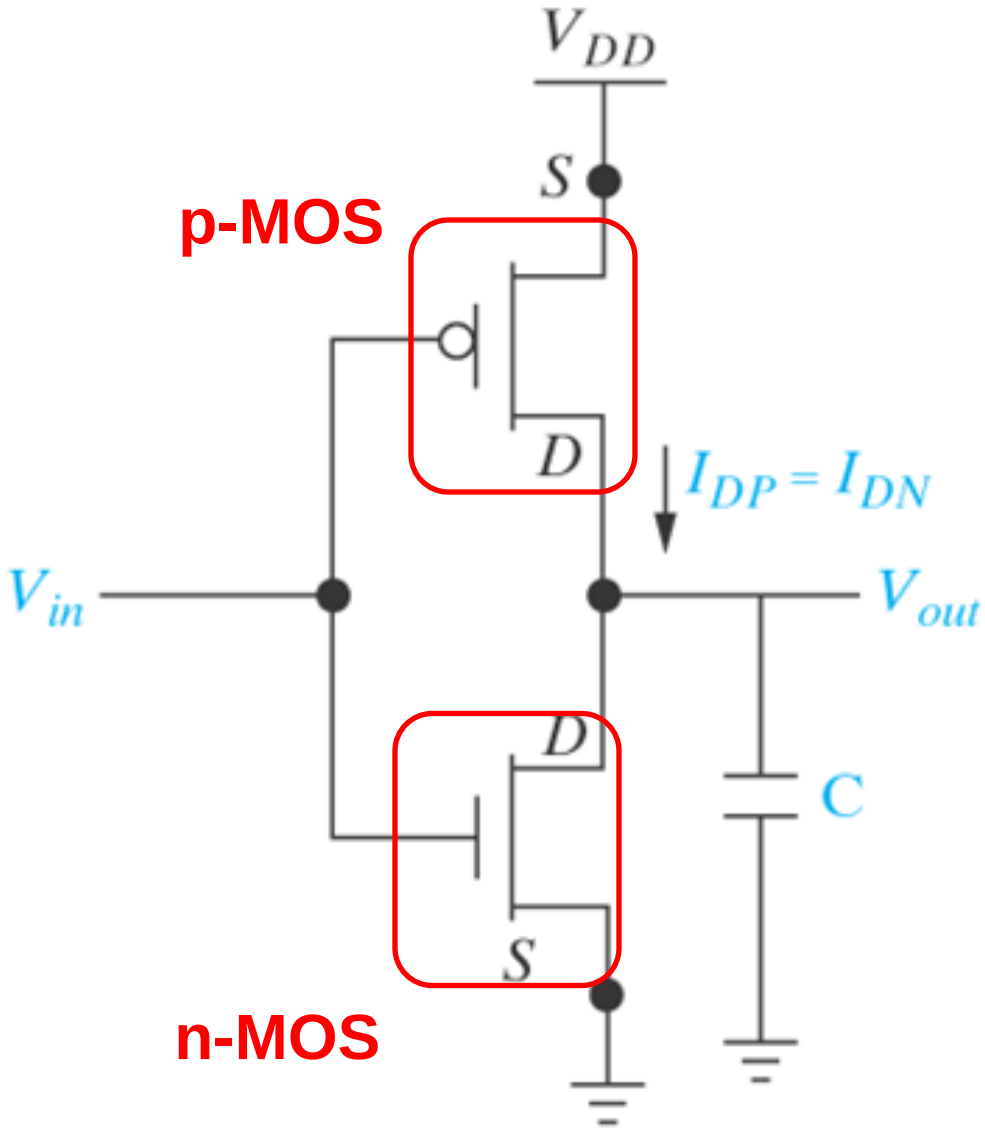
- Power dissipation in resistor
- V_{0L} is not zero



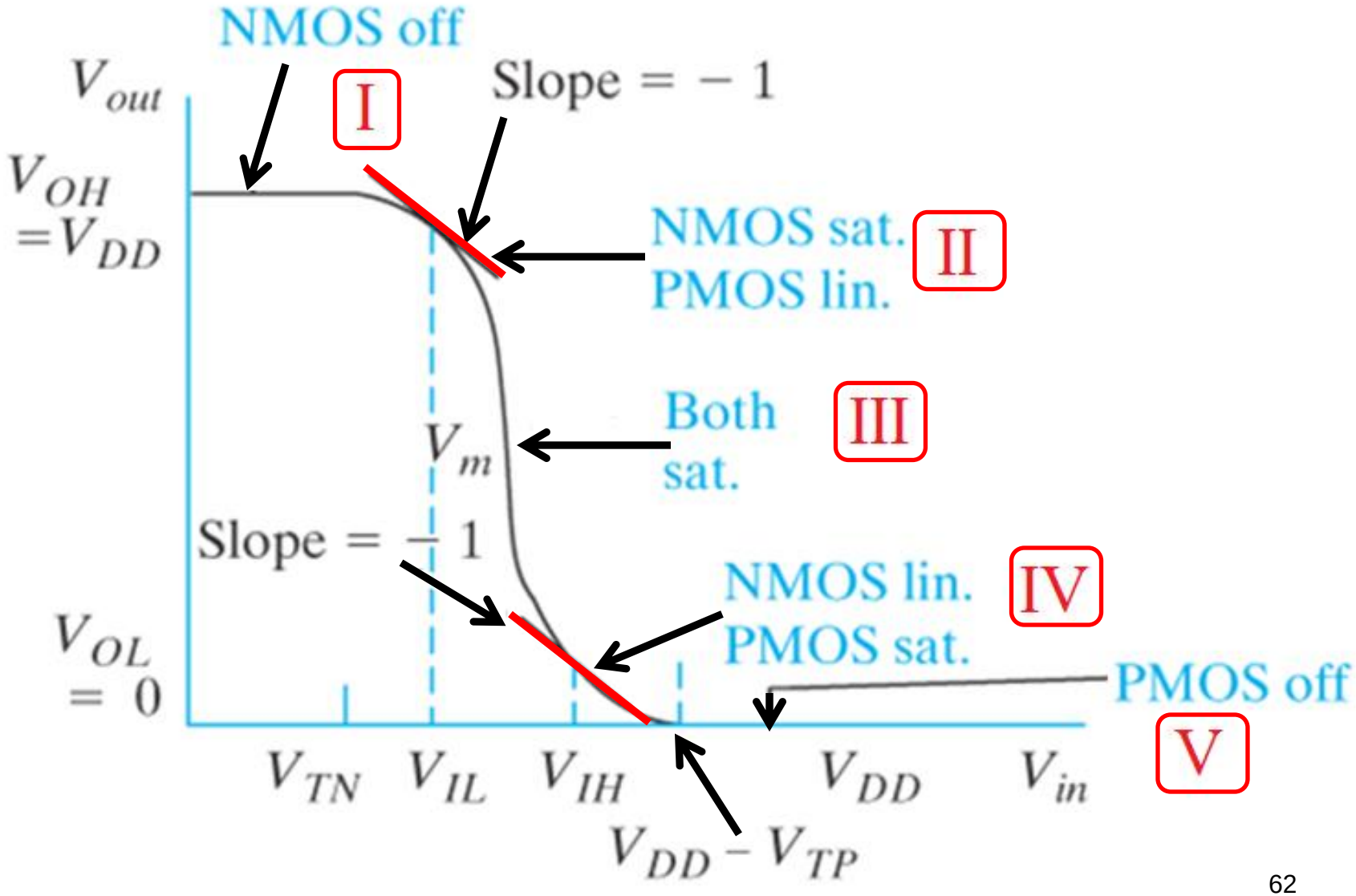
CMOS inverter



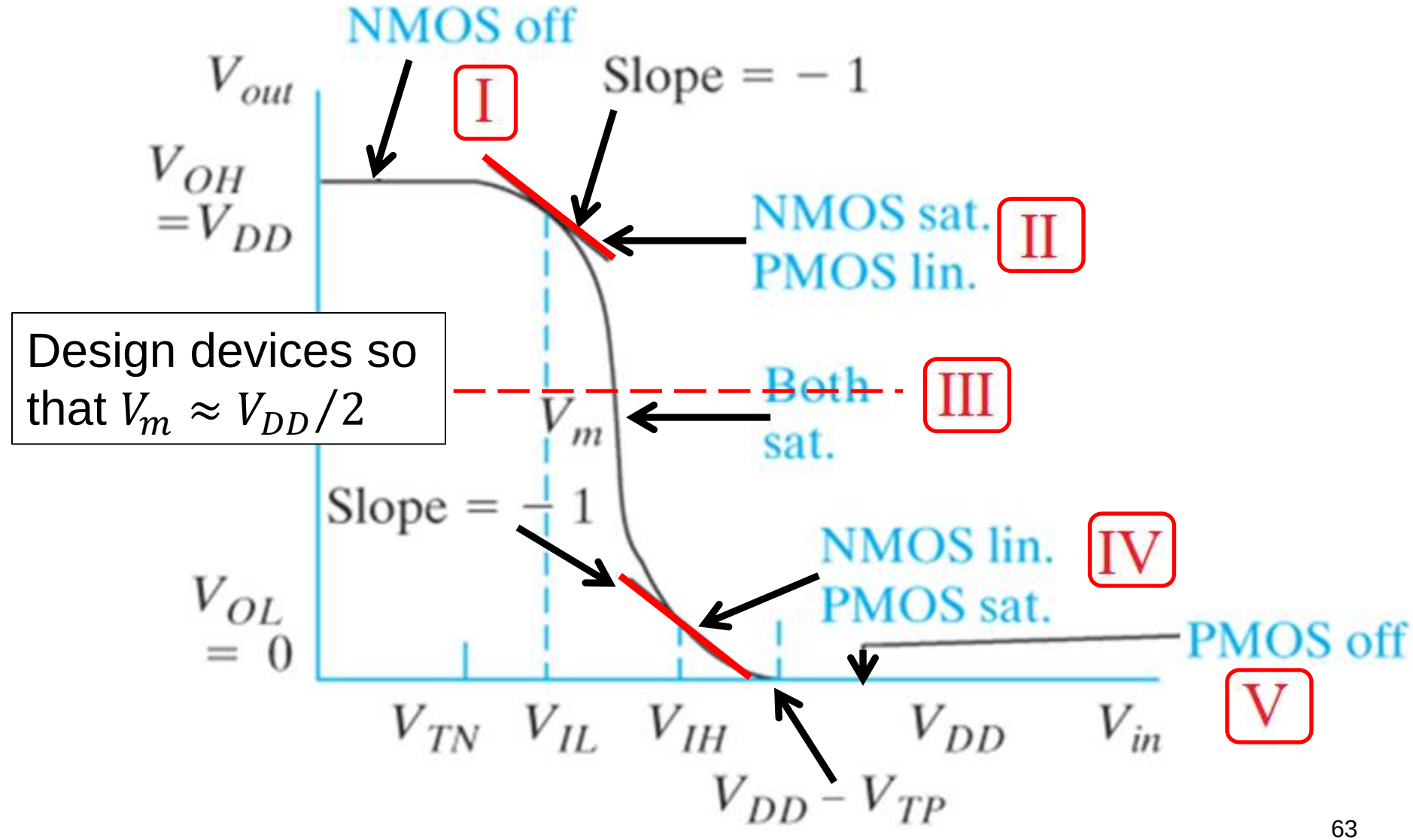
CMOS inverter



CMOS inverter – Voltage transfer characteristics



CMOS inverter – Voltage transfer characteristics



CMOS inverter – Voltage transfer characteristics

Design devices so that $\boldsymbol{V_m \approx V_{DD}/2}$ REGION III

Setting $I_D(\text{NMOSFET}) = I_D(\text{PMOSFET})$

$$\chi = \left(\frac{k_N}{k_P}\right)^{1/2} = \frac{\left[\overline{\mu_n} C_i \left(\frac{Z}{L}\right)_n\right]^{1/2}}{\left[\overline{\mu_p} C_i \left(\frac{Z}{L}\right)_p\right]^{1/2}} = 1$$

CMOS inverter – Voltage transfer characteristics

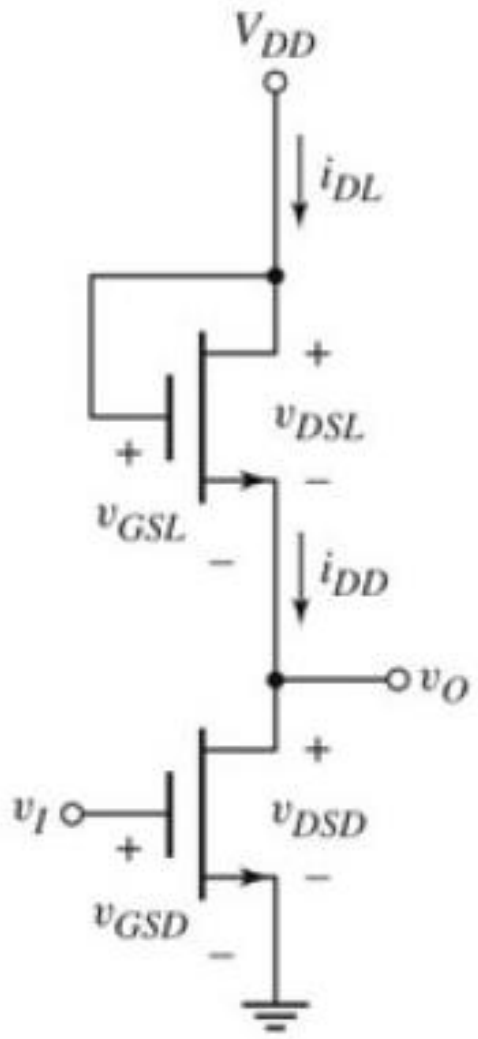
Design devices so that $\boldsymbol{V_m \approx V_{DD}/2}$ REGION III

$$\chi = \left(\frac{k_N}{k_P}\right)^{1/2} = \frac{\left[\overline{\mu_n} C_i \left(\frac{Z}{L}\right)_n\right]^{1/2}}{\left[\overline{\mu_p} C_i \left(\frac{Z}{L}\right)_p\right]^{1/2}} = 1$$

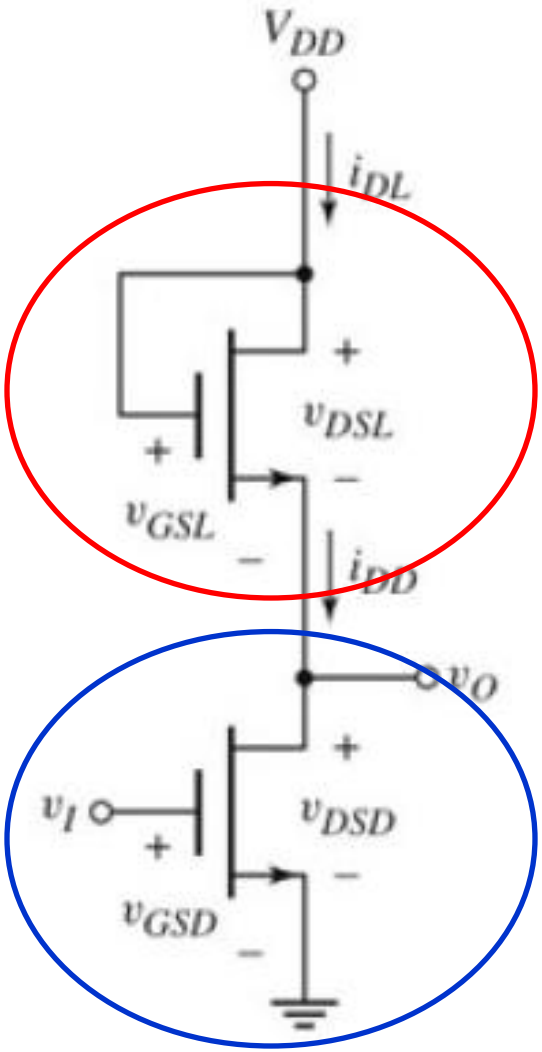
Typically $\overline{\mu_n} \approx 2\overline{\mu_p}$

$$\chi = 1 \rightarrow (Z/L)_p = 2(Z/L)_n$$

Question: Is this a CMOS inverter circuit?



Question: Is this a CMOS inverter?

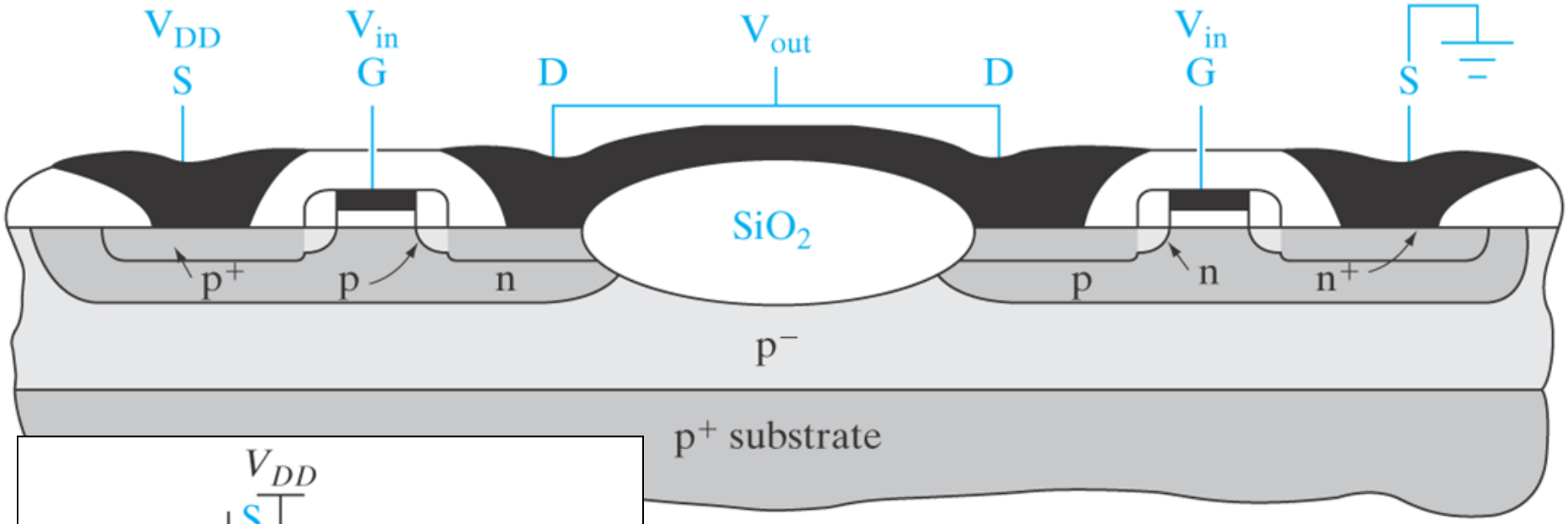


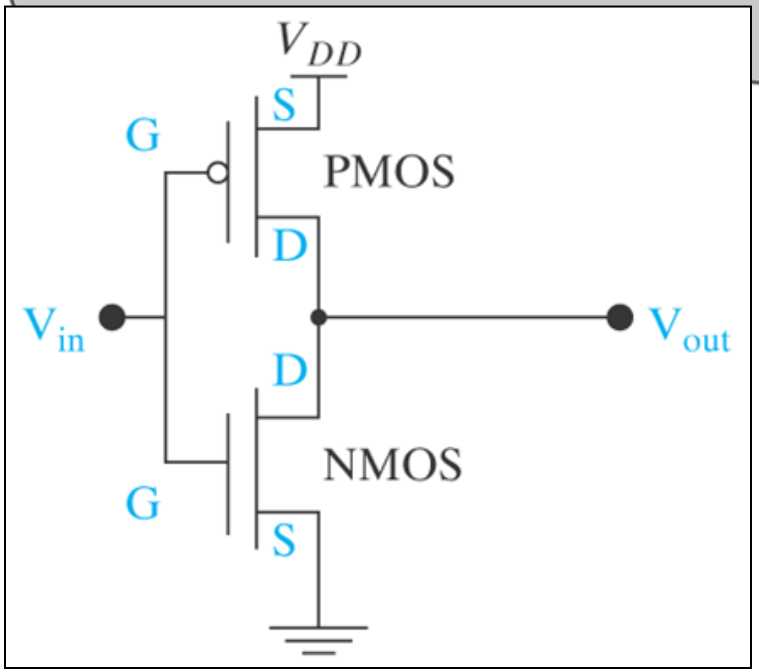
NO!

Both MOS transistors are p-channel and the top one operates in the linear region as a load resistor.

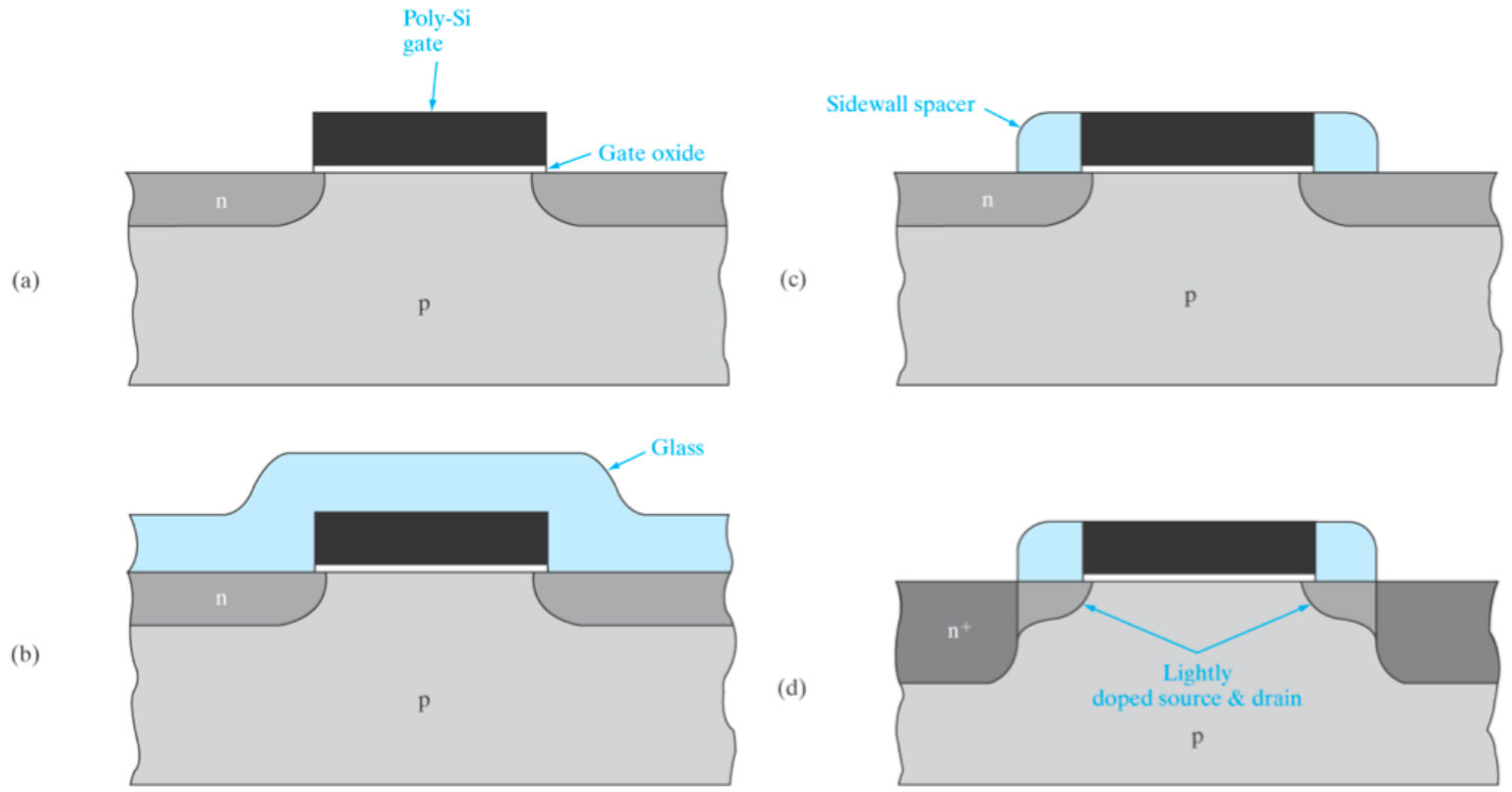
The input is connected only to the gate of this MOS transistor, not to both.

CMOS integration

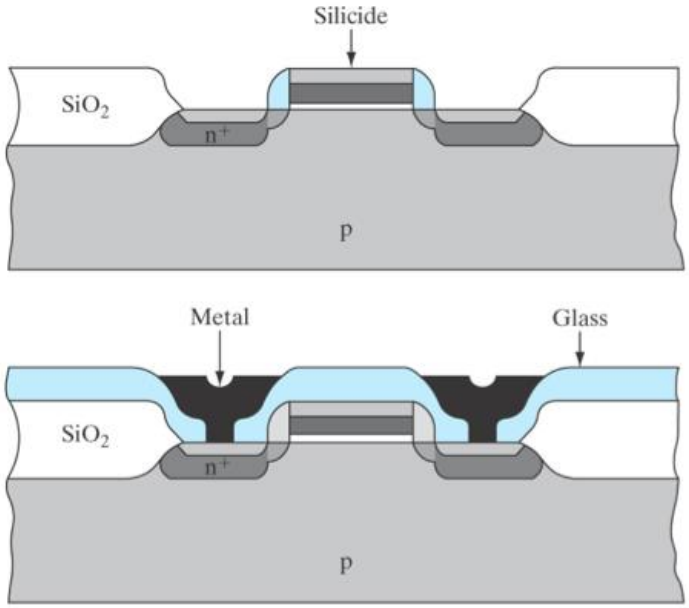




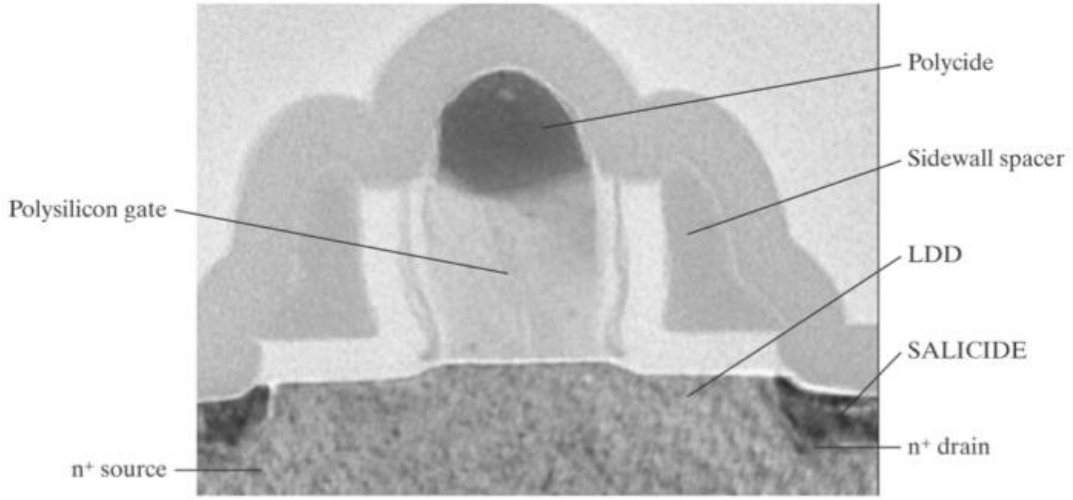
NMOS Fabrication in p-Well



MOSFET – metal contacts



(c)



Multilevel Interconnects